SINO WEALTH

SH67L19

4K 4-bit Micro-controller with LCD Driver

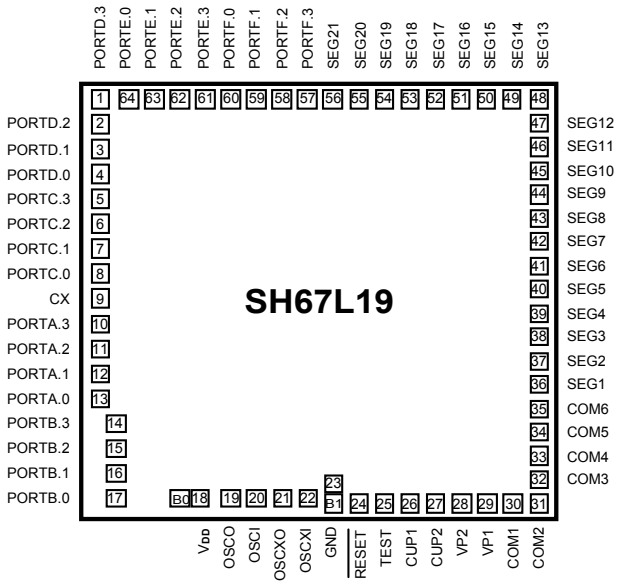
Features

- The SH6610C-based single-chip 4-bit micro-controller with LCD driver
- ROM: 4K X 16 bits
- RAM: 256 X 4 bits
- Operation Voltage: 1.2V - 1.7V
- 4-Level subroutine nesting (include interrupts)
- One 8-bit Timers with pre-divider circuit
- One 8-bit Base Timer
- Warm-up timer for power-on reset
- Powerful interrupt sources:
  - External interrupts (Falling or rising edge)
  - Timer0 interrupts
  - Base Timer interrupts
  - PORTB, C interrupts (Falling or rising edge)
- 24 CMOS bi-directional I/O pins
  - PC, PD, PE, PF can switch to segment
- LCD driver: Up to 6 X 38 dots
  - 1/6 duty, 1/3 bias; 1/5 duty, 1/3 bias; 1/4 duty, 1/3 bias or 1/3 duty, 1/2 bias selected by Code Option
  - 17 segment shared with PORTC, D, E, F and CX
- Built-in voltage double and treble charge pump circuit
- Dual clock sources:
  - OSC: Crystal oscillator: 32.768kHz, RC oscillator: 32kHz or 131kHz. (selected by Code Option)
  - OSCX: Ceramic oscillator: 455kHz, RC oscillator: 262kHz or 500kHz (400kHz - 600kHz). (Selected by system register)
- Instruction cycle time:
  - 122.07μs for 32.768 kHz crystal
  - 30.53μs for 131 kHz RC
  - 8.79μs for 455kHz ceramic
  - 15.27μs for 262kHz RC
  - 8μs for 500kHz RC
- Built-in 2-channel PSG
- Built-in alarm generator
- Built-in EL-light driver
- Built-in watchdog timer
- Built-in Resistor to Frequency converts circuit
- Two low power operation modes: HALT and STOP
- Low power consumption
- Bonding option for multi-code software
- Available in CHIP FORM

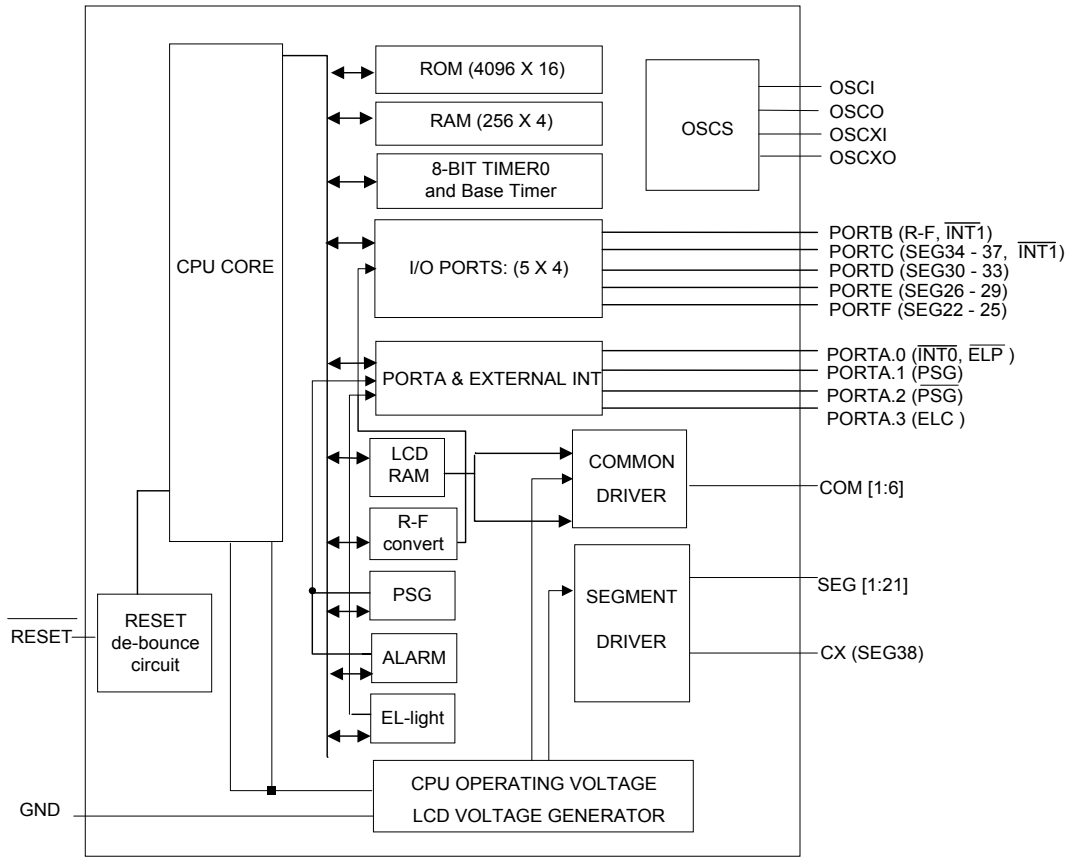
General Description

The SH67L19 is a single chip micro-controller integrated with 4K mask ROM, SRAM, timer, PSG, alarm, RFC, EL-light, LCD driver, I/O ports. This chip builds in a dual-oscillator to enhance the total chip performance.

Pad Configuration



Block Diagram



Pad Description

Pad No.	Designation	I/O	Description
36 - 56	SEG1 - SEG21	O	Segment signal output for LCD display
30 - 35	COM1 - COM6	O	Common signal output for LCD display
29, 28	VP1, VP2	P	Power supply pin for LCD driver
26, 27	CUP1 - 2	P	Connection for voltage doubler capacitor
25	TEST	I	Test pin (Internal pull-low). No connect for user
24	RESET	I	Reset input (internal pull-high selected by Code Option)
18	V_{DD}	P	Power supply
	B0	I	Bonding option, internally pull-low
	B1	I	Bonding option, internally pull-high
23	GND	P	Ground pin
21	OSCXO	O	Oscillator X output
22	OSCXI	I	Oscillator X input
19	OSCO	O	Oscillator output
20	OSCI	I	Oscillator input
10 - 13	PORTA.3 - PORTA.0	I/O	Bit programmable I/O, PORTA.0 could be External Interrupt ($\overline{INT0}$), PORTA.0 input is a schmitt trigger PORTA.0, PORTA.3 could be EL-light output PORTA.0 (ELP), PORTA.3 (ELC) PORTA.1, PORTA.2 could be buzzer output PORTA.1 (PSG), PORTA.2 (/PSG)
14 - 17	PORTB.3 - PORTB.0	I/O	Bit programmable I/O, PORTB could be PORT Interrupt ($\overline{INT1}$) PORTB.0 - PORTB.2 shared with RX1 - 3, PORTB.3 shared with RXB
5 - 8	PORTC.3 - PORTC.0	I/O	Bit programmable I/O, PORTC could be PORT Interrupt ($\overline{INT1}$) PORTC.3 - PORTC.0 shared with LCD Seg34 - 37
1 - 4	PORTD.3 - PORTD.0	I/O	Bit programmable I/O, PORTD.3 - PORTD.0 shared with LCD Seg30 - 33
61 - 64	PORTE.3 - PORTE.0	I/O	Bit programmable I/O, PORTE.3 - PORTE.0 shared with LCD Seg26 - 29
57 - 60	PORTF.3 - PORTF.0	I/O	Bit programmable I/O, PORTF.3 - PORTF.0 shared with LCD Seg22 - 25
9	CX	I/O	R-F converter counter input pin, shared with Seg38

Functional Description

1. CPU

The CPU core contains the following function blocks: Program Counter, ALU, Carry Flag, Accumulator, Table Branch Register (TBR), Data Pointer (INX, DPH, DPM and DPL), and Stack.

1.1. PC (Program Counter)

The PC is used for ROM addressing consisting of 12-bits: Page Register (PC11), and Ripple Carry Counter (PC10 - PC0).

The program counter normally increases by one (+1) with each execution of an instruction except in the following cases:

(1) When executing a jump instruction (such as JMP, BA0, BC),
(2) When executing a subroutine call instruction (CALL),
(3) When an interrupt occurs,
(4) When the chip is at INITIAL RESET.

The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K. Program Counter can only address a 4K of program ROM.

1.2. ALU and CY

The ALU performs arithmetic and logic operations.

It provides the following functions:
Binary addition/subtraction (ADC, SBC, ADD, SUB, ADI, SBI)
Decimal adjustment for addition/subtraction (DAA, DAS),
Logic operations (AND, EOR, OR, ANDIM, EORIM, ORIM)
Decision (BA0, BA1, BA2, BA3, BAZ, BC)
Logic shift (SHR)

The Carry Flag (CY) holds the arithmetic operation ALU overflow.

During interrupt or call instruction, carry is pushed into stack and restored from stack by RTNI. It is unaffected by an RTNW instruction.

1.3. Accumulator

The accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data transfers between the accumulator and system register, LCD RAM, or data memory can be performed.

1.4. Stack

This group of registers is used to save the contents of CY & PC (11 - 0) sequentially with each subroutine call or interrupt. It is organized 13 bits X 4 levels. The MSB is saved for CY. Four levels are the maximum allowed for subroutine calls and interrupts.

The contents of Stack are returned sequentially to the PC with the return instructions (RTNI/RTNW). Stack is operated on a first-in, last-out basis. This 4-level nesting includes both subroutine calls and interrupts requests. Note that program execution may enter an abnormal state if the number of calls and interrupt requests exceeds 4, where then the bottom of stack will be shifted out.

2. ROM

The SH67L19 can address 4K X 16 bit of program area $000 to $FFF. There is an area from addresses $000 through $004 reserved for special interrupts service routines such as starting vector address.

Address	Instruction	Function
000H	JMP Instruction	Jump to RESET service routine
001H	JMP Instruction	Jump to external interrupt service routine ($\overline{INT0}$)
002H	JMP Instruction	Jump to Timer0 service routine
003H	JMP Instruction	Jump to Base Timer service routine
004H	JMP Instruction	Jump to PORTB, C service routine ($\overline{INT1}$)

3. RAM

Built-in SRAM contains general-purpose data memory, LCD RAM, and system registers. Direct addressing in one instruction can access them.

The following is the memory allocation map:

$000 - $01F: System register and I/O
$020 - $11F: Data memory (256 X 4bits, divide into 3 banks)
$300 - $325, $330 - $355: LCD RAM
$360 - $368: PSG control registers (9 X 4 bits)
$269 - $26D: R-F counter registers (5 X 4 bit)

The Configuration of System Register

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks	Initial Value
$00	IEX	IET0	IEBT	IEP	R/W	Interrupt enable flags	0000
$01	IRQX	IRQT0	IRQBT	IRQP	R/W	Interrupt request flags	0000
$02	TM0.3	TM0.2	TM0.1	TM0.0	R/W	Timer0 mode register	0000
$03	BTM.3	BTM.2	BTM.1	BTM.0	R/W	Base timer mode register	0000
$04	T0L.3	T0L.2	T0L.1	T0L.0	R/W	Timer0 load/counter low nibble	0000
$05	T0H.3	T0H.2	T0H.1	T0H.0	R/W	Timer0 load/counter high nibble	0000
$06	ENX	ELON	LCDOFF	PSGON	R/W	Bit0: PSG on/off control Bit1: LCD on/off control Bit2: EL-light on/off control Bit3: R-F convert counter on/off control	0010
$07	O/RF	RX3EN	RX2EN	RX1EN	R/W	Bit0 - 2: count resister1 - 3 enable Bit3: set PORTB as R-F converter	0000
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA data register	0000
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB data register	0000
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC data register	0000
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD data register	0000
$0C	PE.3	PE.2	PE.1	PE.0	R/W	PORTE data register	0000
$0D	PF.3	PF.2	PF.1	PF.0	R/W	PORTF data register	0000
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table branch register	-
$0F	INX.3	INX.2	INX1	INX.0	R/W	Index register (INX)	-
$10	DPL3	DPL2	DPL1	DPL0	R/W	Data pointer for INX low nibble	-
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble	-
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble	-
$13	ELF	ELPF	SOH/L	S/CX	R/W	Bit0: Set CX as LCD segment 38 Bit1: Select LCD segment output high or low EL-LIGHT mode control Bit2: ELP driver output frequency control Bit3: EL-LIGHT driver frequency select	0001
$14	OXS	OXM	OXON	HLM	R/W	Bit0: Heavy Load Mode Bit1: Turn on OSCX oscillator Bit2: CPU clocks select (1: OSCX /0: OSC) Bit3: OSCX type selection	0000

System Register (Cont.)

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks	Initial Value
$15	PULLEN	PH/PL	B1	B0	R/W R	Bit0, 1: Bonding Option Bit2: Port pull high (falling edge interrupt) or pull low (rising edge interrupt) select Bit3: pull high/low enable control	0010
$16	O/S4	O/S3	O/S2	O/S1	R/W	Bit0: Set PORTC as LCD segment Bit1: Set PORTD as LCD segment Bit2: Set PORTE as LCD segment Bit3: Set PORTF as LCD segment	1111
$17	WDT	WT2	WT1	WT0	W	Bit3: WDT time-out bit (write one to reset WDT) Bit2 - 0: Watchdog timer on/off control (initial: 010, watchdog on)	1010
$18	PACR.3	PACR.2	PACR.1	PACR.0	W	Set PORTA to be output port	0000
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	W	Set PORTB to be output port	0000
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	W	Set PORTC to be output port	0000
$1B	-	PFCR	PECR	PDCR	W	Bit0: Set PORTD to be output port Bit1: Set PORTE to be output port Bit2: Set PORTF to be output port	-000
$1C	PCIN	PDIN	PEIN	PFIN	W	When PORTC - PORTF used as input, their input state control Used in key matrix's application	0000
$1D			PAIN	PBIN	W	When PORTA, PORTB used as input, their input state control Used in key matrix's application	--00
$1E - 1F	-	-	-	-		Reserved	
$269	RF1.3	RF1.2	RF1.1	RF1.0	R/W	R-F counter register nibble 1 (bit0 - 3)	0000
$26A	RF2.3	RF2.2	RF2.1	RF2.0	R/W	R-F counter register nibble 2 (bit4 - 7)	0000
$26B	RF3.3	RF3.2	RF3.1	RF3.0	R/W	R-F counter register nibble 3 (bit8 - 11)	0000
$26C	RF4.3	RF4.2	RF4.1	RF4.0	R/W	R-F counter register nibble 4 (bit12 - 15)	0000
$26D	RF5.3	RF5.2	RF5.1	RF5.0	R/W	R-F counter register nibble 5 (bit16 - 19)	0000
$360	C1.3	C1.2	C1.1	C1.0	W	PSG channel 1 low nibble	0000
$361	CM1	C1.6	C1.5	C1.4	W	PSG channel 1high nibble Bit3: channel 1 mode control	0000
$362	C2.3	C2.2	C2.1	C2.0	W	PSG channel 2 nibble 1 or alarm output	0000
$363	C2.7	C2.6	C2.5	C2.4	W	PSG channel 2 nibble 2	0000
$364	C2.11	C2.10	C2.9	C2.8	W	PSG channel 2 nibble 3	0000
$365	CM2	C2.14	C2.13	C2.12	W	PSG channel 2 nibble 4 Bit3: channel 2 mode control	0000
$366	VOL1	VOL0	CH2EN	CH1EN	W	Bit0, Bit1: Channel 1, 2 enable Bit2, Bit3: volume control	0000
$367	P2.1	P2.0	P1.1	P1.0	W	PSG1 and PSG2 Pre-scalar	0000
$368	-	F262	ALM	SEL	W	Bit0: PSG clock source select. Bit1: Alarm on or off. Bit2: OSCX RC oscillator select	0000

4. Data Memory

The general-purpose data memory is organized as 256 X 4 bits. Because of its static feature, the RAM can retain data after the CPU enters STOP or HALT mode.

5. Oscillator Circuit

5.1. Circuit Configuration

The SH67L19 has two on-chip oscillation circuits OSC and OSCX.

OSC is a low frequency crystal (32.768kHz) or RC (32kHz or 131kHz) oscillator determined by the Code Option. This is designed for low frequency operation. OSCX is a high frequency ceramic (455kHz) or RC (262kHz or 500kHz) oscillator. It is designed for high frequency operation.

It is possible to select the high speed CPU processing by a high frequency clock and select low power operation by low operation clock. At the start of reset initialization, OSC is turned on and OSCX is turned off. Immediately after reset initialization, the OSC is automatically selected as the system clock input source.

When starting the reset, the system clock will be set as OSC, and the frequency is 32.768kHz crystal, 32kHz RC or 131kHz RC. After the initialization, users can turn on the OSCX. Then OSC can be switched to OSCX as system clock, and the two-oscillation circuit can be switch randomly. If the OSCX is not used, the OSCXI pin must be connected to GND.

OSC and OSCX will be turned off in STOP mode. When waking up from STOP, the system clock will be set as OSC. After waking up from STOP, the OSC can be switched to OSCX as system clock, if user wants to use high frequency clock.

5.2. Control of Oscillator

The oscillator control register configuration is shown as follows:

Address	Bit3	Bit2	Bit1	Bit0	Remarks
$14	OXS	OXM	OXON	HLM	… Bit1: Turn on OSCX oscillator Bit2: CPU clock select (1: OSCX /0: OSC) Bit3: OSCX type selection

OXON: OSCX oscillation on/off.
0: Turn-off OSCX oscillation 1: Turn-on OSCX oscillation

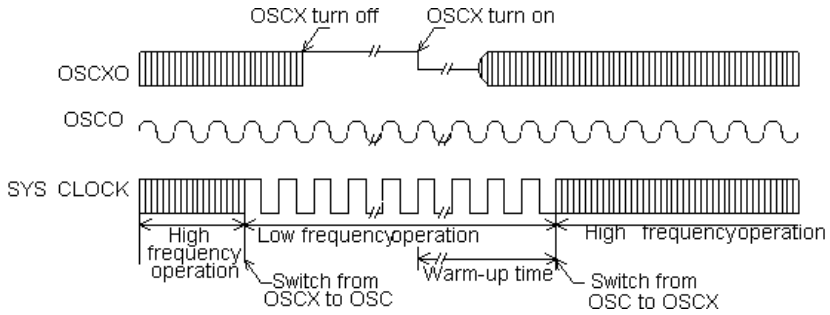
OXM: switching system clock.
0: select OSC as system clock 1: select OSCX as system clock

OXS: OSCX oscillator type selection.
0: OSCX set as Ceramic oscillation 1: OSCX set as RC oscillator

5.3. Programming Notes

It takes at least 5 ms for the OSCX oscillation circuit to turn on until the oscillation stabilizes. When switching the CPU system clock from OSC to OSCX, the user must wait a minimum of 5ms since the OSCX oscillation is running. However, the start time varies with respect to oscillator characteristics and the condition of use. Thus the wait time depends on the application. When switching from OSCX to OSC, and turning off OSCX in one instruction. The OSCX turn off control will be delayed for one instruction cycle automatically to prevent CPU operation error.

5.4. Timing of System Clock Switching



6. System Clock

The system clock varies as the clock source changes. The following table shows the instruction execution time according to each frequency of the system clock source.

	32.768k (OSC)	131k (OSC)	455k (OSCX)	262k (OSCX)	500k (OSCX)
Cycle time	122.07 μs	30.53 μs	8.79 μs	15.27 μs	8 μs

7. I/O PORT

The SH67L19 has 24 CMOS bi-directional I/O ports: PORTA - PORTF. Each I/O pin contains pull-high and pull-low MOS controllable through programming. The PORT control register controls the ON/OFF of the output buffer. I/O ports of the SH67L19 can be accessed by read/write the system register. Users can output any value to any I/O port bit at any time. The circuit configuration of PORTA - F is shown in Figure 1.

7.1. Controlling the Pull-high/Pull-low MOS

PORTA - PORTF contain pull-high/low MOS controlled by the program. System register $15 Bit3, Bit2 controls pull-high/pull-low MOS on or off. Pull-high/pull-low MOS is also controlled by the port data registers of each port as well. Thus the pull-high/pull-low MOS can be turned on/off individually.

Port Mode Register (PMOD)

Address	Bit3	Bit2	Bit1	Bit0	Remarks
$15	PULLEN	PH/PL	B1	B0	… Bit2: Port pull-high/pull-low set Bit3: Port pull-up/pull-low enable control

PULLEN: Pull high/low enable

0: Disable pull-high/low MOS 1: Enable pull-high/low MOS

PH/PL: select pull high or pull low

0: port pull low resistor on 1: port pull high resistor on

7.2. Port Interrupt ($\overline{\text{INT1}}$)

The PORTB and PORTC are used as port interrupt sources (falling or rising edge), only the input port can generate PORT interrupt. When PULLEN = 1, PH/PL = 1 and IEP is set to “1”, any one of the PORTB and PORTC input pin transitions from V_{DD} to GND will generate an interrupt request. When PULLEN = 1, PH/PL = 0 and IEP is set to “1”, any one of the PORTB and PORTC input pin transitions from GND to V_{DD} will generate an interrupt request. When PORTB are used as R-F converter (O/RF = 1), the PORTB interrupt were disabled even the IEP is set to “1”. When PORTC are used as LCD outputs (O/S1 = 1), the PORTC interrupt are disabled also even the IEP is set to “1”.

7.3. External Interrupt ($\overline{INT0}$)

The PORTA.0 is used as external interrupt sources (falling or rising edge), only PORTA.0 is input port can generate an external interrupt. When PULLEN = 1, PH/PL = 1 and IEX is set to “1”, PORTA.0 input pin transitions from V_{DD} to GND will generate an interrupt request. When PULLEN = 1, PH/PL = 0 and IEX is set to “1”, PORTA.0 input pin transitions from GND to V_{DD} will generate an interrupt request. When PORTA.0 is used as ELP, the External interrupt is disabled even the IEX is set to “1”.

Note:

If internal PORT pull-high and pull-low resistor is not used, the SH67L19 will respond PBC or PORTA.0 interrupt by connecting resistors to V_{DD} or GND externally.

7.4. Port I/O Control Register:

Address	Bit3	Bit2	Bit1	Bit0
$18	PACR.3	PACR.2	PACR.1	PACR.0
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0
$1B	-	PFCR	PECR	PDCR

I/O control register: PACR.X - PCCR.X (X = 0, 1, 2, 3) by bit control

1: Defined as an output terminal. 0: Defined as an input terminal (default).

PDCR, PECR, PFCR by port control

1: Defined the port as output terminal. 0: Defined the port as input terminal (default).

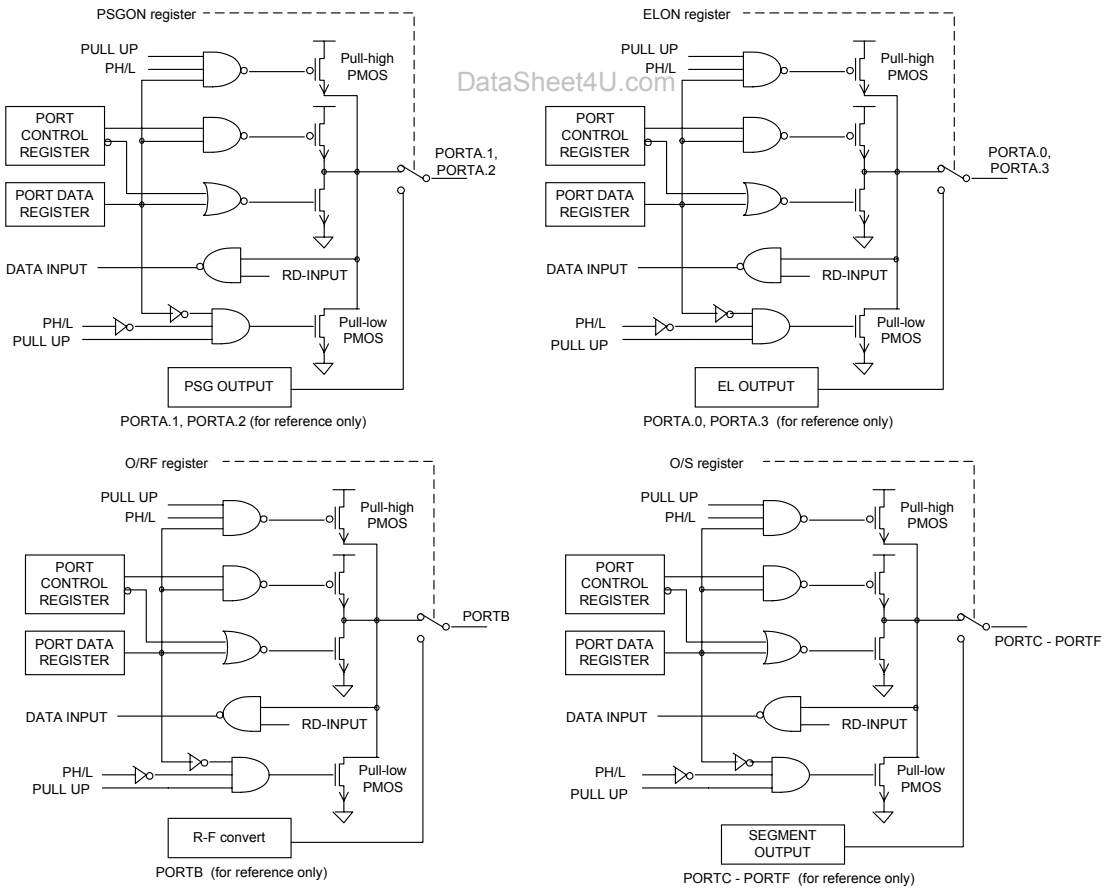


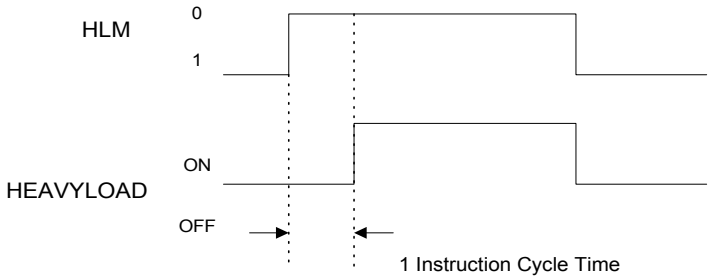
Figure. 1

7.5. Heavy Load Mode (HLM)

Address	Bit3	Bit2	Bit1	Bit0	Remarks
$14	OXS	OXM	OXON	HLM	Bit0: Heavy Load Mode …

HLM: 0 = Heavy load protection mode is released 1 = Heavy load protection mode is set.

The MCU has a heavy load protection circuit when the battery load becomes heavy, such as, when an external buzzer sounds or an external speaker is turned on. In this mode, the low frequency crystal oscillator circuit and high frequency ceramic circuit have been backed up for high gain. When this mode is set, more power would be provided to oscillator circuit. Unless it is necessary, do not set this mode by software since entering the mode would delay an instruction. Please activate the heavy load driving only after setting the HLM for at least one instruction wait cycle through the software. The following shows the programming setting.



7.6. Ports as Key Matrix

The SH67L19's I/O can make up the key matrix and PORTC - PORTF can be used as a LCD segment output at the same time. In this application, users should control that scanning key matrix to share the timing of LCD display and will not affect the LCD display. Only when user scan the key matrix, all Ports are used as I/O; otherwise PORTC - PORTF are used as LCD segment outputs to drive the LCD panel. The Ports used as I/O or segment is controlled by software.

In scan key application, when user doesn't execute the operation of scan key, Ports not sharing the LCD segment output should be set as I/O, and disable it's pull-high/pull-low resistor and input/output access by the corresponding bit of the write system register ($18 - $1D). Executing the above operation can prevent inputting the LCD voltage to the general I/O Ports and the pull-high/pull-low or output of the port affect the LCD segment's waveform.

When users wants to scan key, all ports which make up of the key matrix should be used as general I/O. The ports' pull-high/pull-low resistor and input access should be enabled by clearing the corresponding bit of the system register ($1C, $1D).

Key Matrix's Input Ports Control Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1C	PCIN	PDIN	PEIN	PFIN	W	Control PORTC - PORTF input and output access enable or disable. Used in key matrix's application.
$1D			PAIN	PBIN	W	Control PORTA - PORTB input and output access enable or disable. Used in key matrix's application.

PAIN…PFIN: In the key matrix's application, control PORTA - PORTF input and output access.

0: Enable PORTA - PORTF pull-high/pull-low resistor and I/O access, Ports in normal state

1: Disable PORTA - PORTF pull-high/pull-low resistor and it's I/O access

8. Programmable Sound Generator (PSG)

PSG has channel1 and channel2. Channel 1 is a 7-bit pseudo random counter. Channel 2 is a 15-bit pseudo random counter. Mode bits CM1, CM2 determine which of the two counters will be a noise or a tone generator. To reduce power consumption, disable the sound effect generator during STOP mode. Channel 2 TONE mode is same as Channel 1. (7-bit pseudo-random counter). PSG also provides alarm function. The alarm on or off controlled by register (ALM). This eliminates some programming codes.

Address	Bit 3	Bit 2	Bit 1	Bit 0	Remarks	R/W
$360	C1.3	C1.2	C1.1	C1.0	PSG channel 1 low nibble	W
$361	CM1	C1.6	C1.5	C1.4	PSG channel 1high nibble Bit3: channel 1 mode control	W
$362	C2.3	C2.2	C2.1	C2.0	PSG channel 2 nibble 1 or alarm output	W
$363	C2.7	C2.6	C2.5	C2.4	PSG channel 2 nibble 2	W
$364	C2.11	C2.10	C2.9	C2.8	PSG channel 2 nibble 3	W
$365	CM2	C2.14	C2.13	C2.12	PSG channel 2 nibble 4 Bit3: channel 2 mode control	W
$366	VOL1	VOL0	CH2EN	CH1EN	Bit0: Channel 1 enable Bit1: Channel 2 enable Bit2, Bit3: volume control (initially 0, no sound)	W
$367	P2.1	P2.0	P1.1	P1.0	PSG1 and PSG2 Pre-scalar	W
$368	-	F262	ALM	SEL	Bit0: PSG clock source select. Bit1: Alarm on or off. Bit2: OSCX RC oscillator select	W

PORTA.1 and PORTA.2 Output Control and Vol. Control

When PSGON = 1 and ALM=0, the PORTA.1 PORTA.2 is used as PSG output and controlled by the volume control bit into 4 volume levels output. When PSGON = 1 and ALM = 1, the alarm function will open, PORTA.1 PORTA.2 is used as alarm output.

PSGON	ALM	Function
0	X	PORTA.1 and PORTA.2 as I/O Port
1	0	PORTA.1 and PORTA.2 as PSG output
1	1	PORTA.1 and PORTA.2 as Alarm output

VOL1	VOL0	Vol. Level
0	0	1 (no sound)
0	1	2
1	0	3
1	1	4

PSG Two Channels Mode Control

When using PSG output (PSGON = 1 and ALM = 0), two channels' mode is controlled by CM1 ($361 bit3), CM2 ($365 bit3):
CM1: 1: channel 1 is noise generator. 0: channel 1 is tone generator.
CM2: 1: channel 2 is noise generator. 0: channel 2 is tone generator.

Channel 1

Channel 1 is constructed by a 7-bit pseudo random counter. Channel 1 is enabled/disabled by CH1EN. It can be a 7-bit wide-band noise generator or a 7-bit sound generator. It can create either sound frequency by writing value N in C1.6 - C1.0.

Channel 2

Channel 2 is constructed by a 15-bit pseudo random counter. Channel 2 is enabled/disabled by CH2EN. It can be a 15-bit wide-band noise generator or a 7-bit sound generator. It can create either sound frequency by writing value N in C2.8 - C2.14.

PSG Clock Control Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	Remarks
$367	P2.1	P2.0	P1.1	P1.0	PSG1 and PSG2 Pre-scalar
$368	-	F262	ALM	SEL	Bit0: PSG clock source select Bit1: Alarm on or off Bit2: OSCX RC oscillator select

P1.0, P1.1 and P2.0, P2.1 select the pre-scalar of PSG actual clock

P1.1, P2.1	P1.0, P2.0	Pre-scalar Divide Ratio	Clock Source	Actual Clock
0	0	1	32 kHz	32 kHz
0	1	2	32 kHz	16 kHz
1	0	4	32 kHz	8 kHz
1	1	8	32 kHz	4 kHz

SEL: select OSC or OSCX is used to generate PSG clock source

0: PSG clock source is provided by OSC (low frequency clock)

1: PSG clock source is provided by OSCX (high frequency clock)

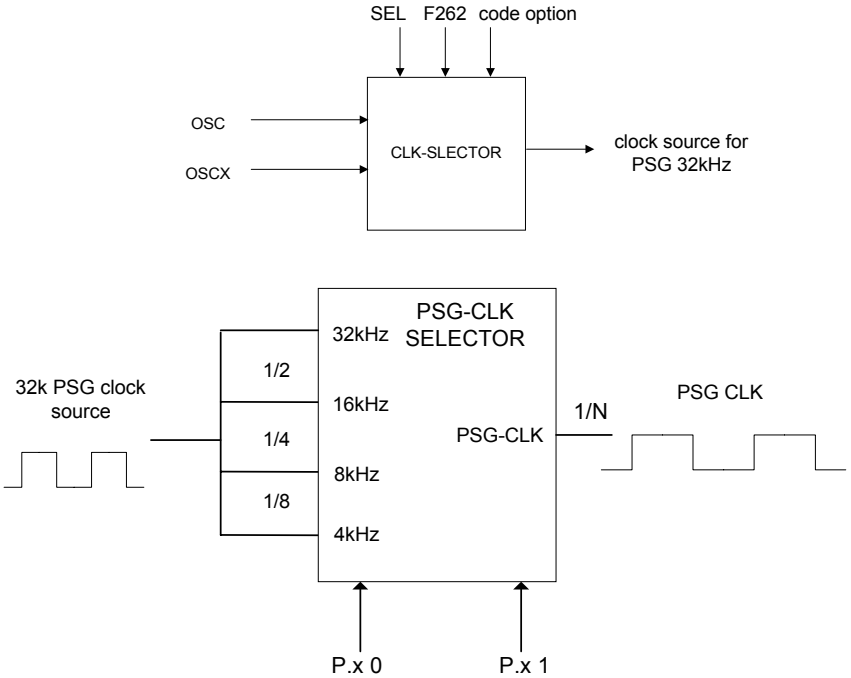
F262: OSCX RC oscillator frequency selection

0: Use 500k RC as oscillator

1: Use 262k RC as oscillator

If the OSCX is used as system clock, the value of bit “F262” must correspond to the OSCX’s frequency, otherwise PSG clock source will not be true. No matter which oscillator and frequency is selected to provide PSG clock source, the PSG clock source is always equal 32kHz.

PSG Sub-Block Diagram:



Example:

A user uses 500kHz RC clock, and wants to create a tone 'C3' whose frequency are 130.81Hz.
If the user writes 00H to P.1 and P.0, and sets OXON, OXM, OXS = 1, so that the system clock is 500kHz, PSG clock source is 32kHz and PSG-CLK = 32kHz, the value of N is 32k/130.81/2 = 122.3, looking up 122 in the table, and the corresponding initial data of LSFR is 20H.
If the user writes 01H to P.1 and P.0, then the PSG-CLK is 16kHz, the value of N is 16k/130.81/2 = 61.2, and the initial data is 49H.
If the user writes 10H to P.1 and P.0, then the PSG-CLK is 8kHz, the value of N is 8k/130.81/2 = 31, and the initial data is 4BH.
If the user writes 11H to P.1 and P.0, then the PSG-CLK is 4kHz, the value of N is 4k/130.81/2 = 15, and the initial data is 15H.
When the tone frequency is too low, the expected value of N maybe greater than 127, and the counter cannot create such value. A better way is to select a low PSG-CLK. For example, for the frequency of tone 'C1' is 32.7Hz, if the PSG-CLK is greater than 8kHz, the expected N is greater than 127, but the 4kHz PSG-CLK can create this tone.
According to the previous illustration, users can make a music table by themselves. If a user selects any oscillator and PSG-CLK, the music table is given as follows.

Music Table1:

Following is the music scale reference table for channel 1(or channel 2) under Actual Clock = 32kHz.

Note	Ideal freq.	N	LSFR (C1.6 - C1.0) (C2.14 - C2.8)	Real freq.	Error %	Note	Ideal freq.	N	LSFR (C1.6 - C1.0) (C2.14 - C2.8)	Real freq.	Error %
C3	130.81	122	20	131.15	0.26%	G4	392.0	41	58	390.24	-0.44%
D3	146.83	109	51	146.79	-0.03%	A4	440.0	36	1A	444.44	1.01%
E3	164.81	97	45	164.95	0.08%	B4	493.9	32	25	500.00	1.24%
F3	174.61	92	33	173.91	-0.40%	C5	523.2	31	4B	516.13	-1.36%
G3	195.99	82	27	195.12	-0.44%	D5	587.3	27	3B	592.59	0.90%
A3	220.00	73	21	219.18	-0.37%	E5	659.2	24	5C	666.67	1.13%
B3	246.94	65	44	246.15	-0.32%	F5	698.4	23	39	695.65	-0.40%
C4	261.62	61	49	262.30	0.26%	G5	784.0	20	4C	800.00	2.04%
D4	293.66	54	5A	296.30	0.90%	A5	880.0	18	32	888.89	1.01%
E4	329.62	49	5B	326.53	-0.94%	B5	987.7	16	4A	1000.00	1.24%
F4	349.22	46	5E	347.83	-0.40%	C6	1046.5	15	15	1066.67	1.93%

Music Table2:

Following is the music scale reference table for channel 1(or channel 2) under Actual Clock = 16kHz.

Note	Ideal freq.	N	LSFR (C1.6 - C1.0) (C2.14 - C2.8)	Real freq.	Error %	Note	Ideal freq.	N	LSFR (C1.6 - C1.0) (C2.14 - C2.8)	Real freq.	Error %
C2	65.41	122	20	65.57	0.26%	G3	195.99	41	58	195.12	-0.44%
D2	73.41	109	51	73.39	-0.03%	A3	220.00	36	1A	222.22	1.01%
E2	82.41	97	45	82.47	0.08%	B3	246.94	32	25	250.00	1.24%
F2	87.31	92	33	86.96	-0.40%	C4	261.62	31	4B	258.06	-1.36%
G2	98.00	82	27	97.56	-0.44%	D4	293.66	27	3B	296.30	0.90%
A2	110.00	73	21	109.59	-0.37%	E4	329.62	24	5C	333.33	1.13%
B2	123.47	65	44	123.08	-0.32%	F4	349.22	23	39	347.83	-0.40%
C3	130.81	61	49	131.15	0.26%	G4	391.99	20	4C	400.00	2.04%
D3	146.83	54	5A	148.15	0.90%	A4	439.99	18	32	444.44	1.01%
E3	164.81	49	5B	163.27	-0.94%	B4	493.87	16	4A	500.00	1.24%
F3	174.61	46	5E	173.91	-0.40%	C5	523.24	15	15	533.33	1.93%

Music Table3:

Following is the music scale reference table for channel 1(or channel 2) under Actual Clock = 8kHz.

Note	Ideal freq.	N	LSFR (C1.6 - C1.0) (C2.14 - C2.8)	Real freq.	Error %	Note	Ideal freq.	N	LSFR (C1.6 - C1.0) (C2.14 - C2.8)	Real freq.	Error %
C1	32.70	122	20	32.79	0.26%	G2	98.00	41	58	97.56	-0.44%
D1	36.71	109	51	36.70	-0.03%	A2	110.00	36	1A	111.11	1.01%
E1	41.20	97	45	41.24	0.08%	B2	123.47	32	25	125.00	1.24%
F1	43.65	92	33	43.48	-0.40%	C3	130.81	31	4B	129.03	-1.36%
G1	49.00	82	27	48.78	-0.44%	D3	146.83	27	3B	148.15	0.90%
A1	55.00	73	21	54.79	-0.37%	E3	164.81	24	5C	166.67	1.13%
B1	61.73	65	44	61.54	-0.32%	F3	174.61	23	39	173.91	-0.40%
C2	65.41	61	49	65.57	0.26%	G3	195.99	20	4C	200.00	2.04%
D2	73.41	54	5A	74.07	0.90%	A3	220.00	18	32	222.22	1.01%
E2	82.41	49	5B	81.63	-0.94%	B3	246.94	16	4A	250.00	1.24%
F2	87.31	46	5E	86.96	-0.40%	C4	261.62	15	15	266.67	1.93%

Music Table4:

Following is the music scale reference table for channel 1(or channel 2) under Actual Clock = 4kHz.

Note	Ideal freq.	N	LSFR (C1.6 - C1.0) (C2.14 - C2.8)	Real freq.	Error %	Note	Ideal freq.	N	LSFR (C1.6 - C1.0) (C2.14 - C2.8)	Real freq.	Error %
C0	16.35	122	20	16.39	0.26%	G1	49.00	41	58	48.78	-0.44%
D0	18.35	109	51	18.35	-0.03%	A1	55.00	36	1A	55.56	1.01%
E0	20.60	97	45	20.62	0.08%	B1	61.73	32	25	62.50	1.24%
F0	21.83	92	33	21.74	-0.40%	C2	65.41	31	4B	64.52	-1.36%
G0	24.50	82	27	24.39	-0.44%	D2	73.41	27	3B	74.07	0.90%
A0	27.50	73	21	27.40	-0.37%	E2	82.41	24	5C	83.33	1.13%
B0	30.87	65	44	30.77	-0.32%	F2	87.31	23	39	86.96	-0.40%
C1	32.70	61	49	32.79	0.26%	G2	98.00	20	4C	100.00	2.04%
D1	36.71	54	5A	37.04	0.90%	A2	110.00	18	32	111.11	1.01%
E1	41.20	49	5B	40.82	-0.94%	B2	123.47	16	4A	125.00	1.24%
F1	43.65	46	5E	43.48	-0.40%	C3	130.81	15	15	133.33	1.93%

The value N of divider1 is corresponding to the REG C1.6 - C1.0 or REG C2.14 - C2.8 as shown in the following table:

LSFR (C1.6 - C1.0) (C2.14 - C2.8)	N	LSFR (C1.6 - C1.0) (C2.14 - C2.8)	N	LSFR (C1.6 - C1.0) (C2.14 - C2.8)	N	LSFR (C1.6 - C1.0) (C2.14 - C2.8)	N
01	127	16	95	12	63	4B	31
02	126	2C	94	24	62	17	30
04	125	59	93	49	61	2E	29
08	124	33	92	13	60	5D	28
10	123	67	91	26	59	3B	27
20	122	4E	90	4D	58	77	26
41	121	1D	89	1B	57	6E	25
03	120	3A	88	36	56	5C	24
06	119	75	87	6D	55	39	23
0C	118	6A	86	5A	54	73	22
18	117	54	85	35	53	66	21
30	116	29	84	6B	52	4C	20
61	115	53	83	56	51	19	19
42	114	27	82	2D	50	32	18
05	113	4F	81	5B	49	65	17
0A	112	1F	80	37	48	4A	16
14	111	3E	79	6F	47	15	15
28	110	7D	78	5E	46	2A	14
51	109	7A	77	3D	45	55	13
23	108	74	76	7B	44	2B	12
47	107	68	75	76	43	57	11
0F	106	50	74	6C	42	2F	10
1E	105	21	73	58	41	5F	9
3C	104	43	72	31	40	3F	8
19	103	07	71	63	39	7F	7
72	102	0E	70	46	38	7E	6
64	101	1C	69	0D	37	7C	5
48	100	38	68	1A	36	78	4
11	99	71	67	34	35	70	3
22	98	62	66	69	34	60	2
45	97	44	65	52	33	40	1
0B	96	09	64	25	32		

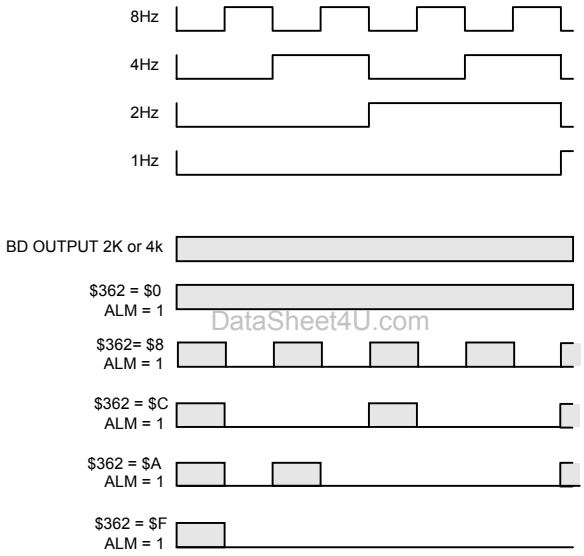
Alarm Generator Mode:

When PSGON = 1 and ALM = 1, the circuit will provide the alarm carrier frequency (4kHz or 2 kHz selected by Code Option) and Channel 2 will provide the alarm envelope signal. The channel 2 low nibble C2.0 - C2.3 will be the alarm control register.

Alarm control register ($362):

C2.3	C2.2	C2.1	C2.0	Alarm output control
0	0	0	0	DC envelop
X	X	X	1	1Hz output
X	X	1	X	2Hz output
X	1	X	X	4Hz output
1	X	X	X	8Hz output

The programming alarm waveform is shown below:



9. Timer 0

The SH67L19 has one 8-bit timer. The timer consists of an 8-bit up counter and an 8-bit preload register.

The timers provide the following functions:

- Programmable internal timer function
- Read the counter values

9.1. Timer 0 Configuration and Operation

The timer 0 consists of an 8-bit write-only timer load register (TL0L, TL0H) and an 8-bit read-only timer counter (TC0L, TC0H). Each has low order digits and high order digits. Writing data into the timer load register (TL0L, TL0H) can initialize the timer counter. Write the low-order digit first and then the high-order digit. The timer counter is loaded with the content of the load register automatically when the high order digit is written or counts overflow happens. The timer overflow will generate an interrupt, if the interrupt enable flag is set.

The timer can be programmed in several different system clock sources by setting the Timer Mode register (TM0).

Timer 0 reads and writes operations follow these rules:

Write Operation	Read Operation
Low nibble first	High nibble first
High nibble to update the counter	Low nibble follows

9.2. Timer0 Mode Register (TM0)

The 8-bit counter counts pre-scaler overflow output pulses. TM0 are 4-bit registers used for timer control as shown in Table 1.2

When the OSC used as system clock, the timer0's clock source can't be selected by TM0.3, the timer0's clock source is system clock (OSC/4). See in Table1.

Table 1. Timer0 Mode Registers ($02)

TM0.3	TM0.2	TM0.1	TM0.0	Prescaler	Clock Source
0	0	0	0	/2048	System clock
0	0	0	1	/512	System clock
0	0	1	0	/128	System clock
0	0	1	1	/32	System clock
0	1	0	0	/8	System clock
0	1	0	1	/4	System clock
0	1	1	0	/2	System clock
0	1	1	1	/1	System clock

When the OSCX is used as system clock, the TM0.3 can select timer0's clock source. See in Table 2
TM0.3 = 0: timer0 clock source is system clock (OSCX/4)
TM0.3 = 1: timer0 clock source is generated by OSC; clock source is 32k (32.768kHz crystal, 32kHz RC or RC 131kHz/4)

Table 2. Timer0 Mode Registers ($02)

TM0.3	TM0.2	TM0.1	TM0.0	Prescaler	Clock Source
0	0	0	0	/2048	System clock
0	0	0	1	/512	System clock
0	0	1	0	/128	System clock
0	0	1	1	/32	System clock
0	1	0	0	/8	System clock
0	1	0	1	/4	System clock
0	1	1	0	/2	System clock
0	1	1	1	/1	System clock
1	0	0	0	/2048	32k
1	0	0	1	/512	32k
1	0	1	0	/128	32k
1	0	1	1	/32	32k
1	1	0	0	/8	32k
1	1	0	1	/4	32k
1	1	1	0	/2	32k
1	1	1	1	/1	32k

9.3. Warm-up Counter

In 32k RC mode, the warm-up counter prescaler is divided by 2^{10} (1024)
In 131k RC mode, the warm-up counter prescaler is divided by 2^{12} (4096)
In CRYSTAL mode, the warm-up counter prescaler is divided by 2^{13} (8192)

10. Base Timer

The MCU has a base timer. The base timer clock source is 32k (32.768kHz crystal, 32kHz RC or RC 131kHz/4). After MCU is reset, it counts at every clock-input signal. When it counts to $FF, right after next clock input, the counter counts to $00 and generates an overflow.

This causes the interrupt of base timer interrupt request flag to 1.Therefore, the base timer can function as an interval timer periodically, generating overflow output as every 256th clock signal output.

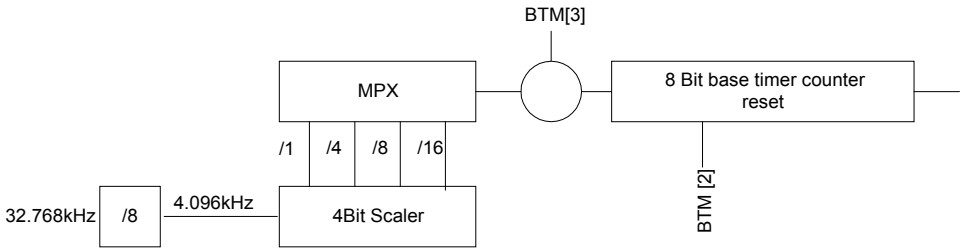
The timer accepts 4kHz clock, and base timer generates an accurate timing interrupt.

This clock-input source is selected by BTM register.

Address	Bit3	Bit2	Bit1	Bit0	Remarks
$03	BTM.3	BTM.2	BTM.1	BTM.0	Base timer mode register

BTM.3 = 0: Disable the base timer BTM.3 = 1: Enable the base timer

BTM.2 = 0: Non reset the base timer BTM.2 = 1: reset the base timer



BTM.1	BTM.0	Prescaler Ratio	Clock Source
0	0	/1	4.096kHz
0	1	/4	4.096kHz
1	0	/8	4.096kHz
1	1	/16	4.096kHz

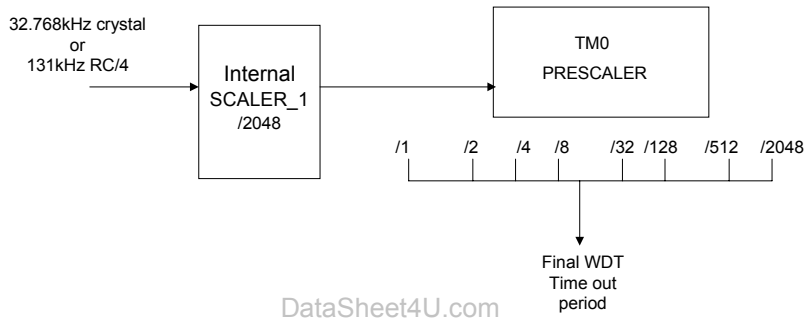
11. Watchdog Timer

The SH67L19 has a Watchdog-Timer. The input clock of the watchdog timer is fetched from the low frequency oscillator (OSC). So the WDT will not run in the STOP mode. The SH67L19 will generate a RESET condition when the Watchdog timing-out. The Watchdog can be enabled or disabled permanently by the system register ($17)'s bit2 - 0. To prevent it from timing-out and generating a device RESET condition, users should write bit3 of system register $17 as "1" before timing-out. If a longer timing-out period is desired, a prescaler with a division ratio of up to 1:2048 can be assigned to the WDT under software controlled by writing to the TM0 register ($02).

System Register $17

Address	Bit 3	Bit 2	Bit 1	Bit 0	Remarks	Power On
$17	WDT	WT2	WT1	WT0	Bit3: Watchdog timer reset/flag. (write 1 to reset WDT) Bit2 - 0: Watchdog timer on/off control	1010

WT2 - WT0 = 010 (defualt), 000, 001, 011, 100 110, 111: watchdog timer is enabled
WT2 - WT0 = 101: watchdog timer is disable



Prescaler Divide Ratio:

TM0.2	TM0.1	TM0.0	Prescaler Divide Ratio	Time out Period
1	1	1	1:1	64ms
1	1	0	1:2	128ms
1	0	1	1:4	256ms
1	0	0	1:8	512ms
0	1	1	1:32	2048ms
0	1	0	1:128	8192ms
0	0	1	1:512	32768ms
0	0	0	1:2048 (Power on initial)	131072ms

12. LCD Driver

The LCD driver contains a controller, a voltage generator, 6 common signal pins and up to 38 segment driver pins. There are three different driving modes: 1/6 duty and 1/3 bias, 1/5 duty and 1/3 bias, 1/4 duty and 1/3 bias, 1/3 duty and 1/2 bias. The driving mode is controlled by Code Option. Also PORTC - PORTF can be used as LCD segment (selected by system register).

When the "STOP" instruction is executed, the LCD will be turned off, but the data of LCD RAM is the same as that before the "STOP" instruction is executed. When the LCD is off, both COMMON and SEGMENT output high or low. The OSC will always be the source clock for LCD frame frequency, no matter the CPU system clock is OSC or OSCX.

12.1. LCD Control Register

Address	Bit3	Bit2	Bit1	Bit0	Remarks	Power On
$06	ENX	ELON	LCDOFF	PSGON	… Bit1: LCD on/off control …	0010
$13	ELF	ELPF	SOH/L	S/CX	Bit0: Select CX or LCD segment38 Bit1: Select LCD segment output high or low …	0001
$16	O/S4	O/S3	O/S2	O/S1	Bit0: Select PORTC or LCD segment Bit1: Select PORTD or LCD segment Bit2: Select PORTE or LCD segment Bit3: Select PORTF or LCD segment	1111

LCDOFF: 0: LCD on and pump on 1:LCD off

SOH/L: 0: When LCD off, COM and SEG output low
1: When LCD off, COM and SEG output high

S/CX: 0: CX 1: SEG38

O/S4: 0: PORTF as I/O 1: PORTF as segment 22 - 25

O/S3: 0: PORTE as I/O 1: PORTE as segment 26 - 29

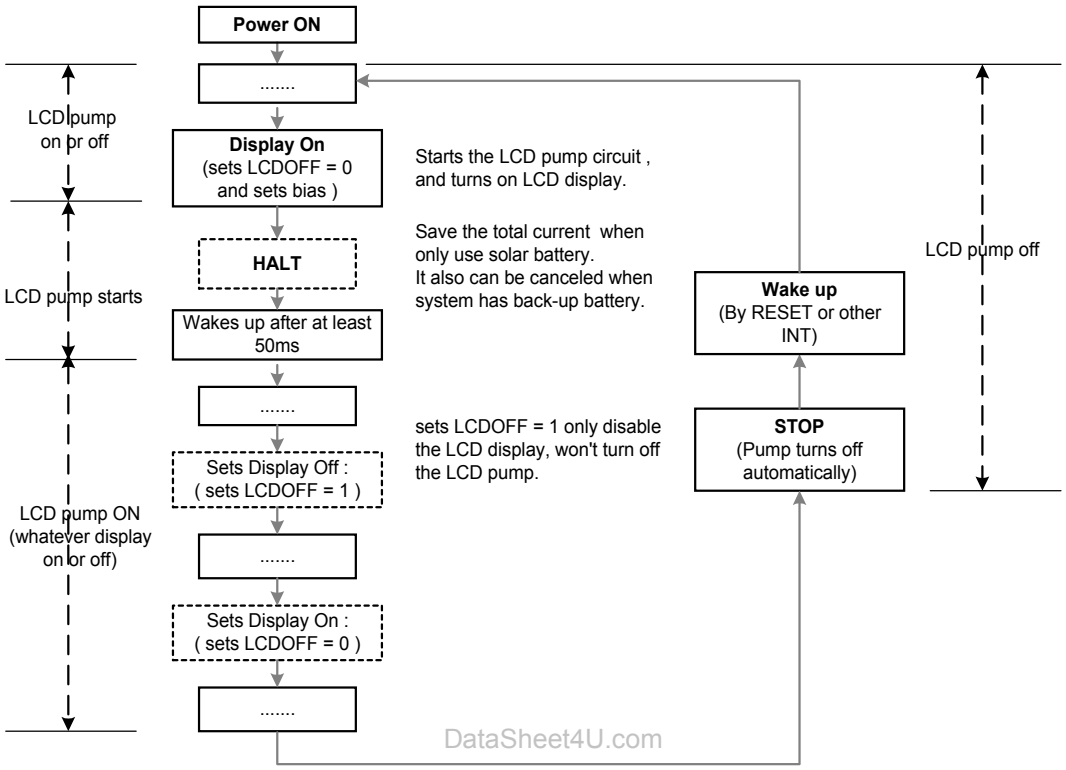
O/S2: 0: PORTD as I/O 1: PORTD as segment 30 - 33

O/S1: 0: PORTC as I/O 1: PORTC as segment 34 - 37

Notice:

1. The LCDOFF (system register 06H bit1) will be set to “1” after reset, and the LCD display will be disabled.
2. The LCD pump circuit may be on or off after Power-on Reset. When LCDOFF (system register $06 bit1) is cleared to “0”, the LCD pump circuit will be turned on. It will turn off only after receiving a “STOP” instruction.
3. Setting LCDOFF = 1 disables the LCD display output only, and won’t turn off the LCD pump circuit.
4. When the SH67L19 runs in STOP mode, the LCD pump circuit turns off automatically. The user should turn on the LCD pump (set LCDOFF = 0) after the next wake up.

Example:



12.2. Configuration of LCD RAM

LCD 1/6 duty, 1/3 bias (COM1 - 6, SEG1 - 38)

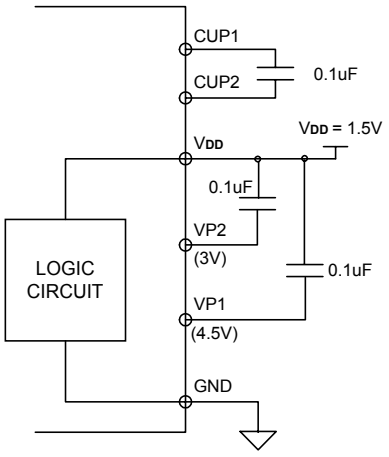
Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM4	COM3	COM2	COM1		-	-	COM6	COM5
300H	SEG1	SEG1	SEG1	SEG1	330H	-	-	SEG1	SEG1
301H	SEG2	SEG2	SEG2	SEG2	331H	-	-	SEG2	SEG2
302H	SEG3	SEG3	SEG3	SEG3	332H	-	-	SEG3	SEG3
303H	SEG4	SEG4	SEG4	SEG4	333H	-	-	SEG4	SEG4
304H	SEG5	SEG5	SEG5	SEG5	334H	-	-	SEG5	SEG5
305H	SEG6	SEG6	SEG6	SEG6	335H	-	-	SEG6	SEG6
306H	SEG7	SEG7	SEG7	SEG7	336H	-	-	SEG7	SEG7
307H	SEG8	SEG8	SEG8	SEG8	337H	-	-	SEG8	SEG8
308H	SEG9	SEG9	SEG9	SEG9	338H	-	-	SEG9	SEG9
309H	SEG10	SEG10	SEG10	SEG10	339H	-	-	SEG10	SEG10
30AH	SEG11	SEG11	SEG11	SEG11	33AH	-	-	SEG11	SEG11
30BH	SEG12	SEG12	SEG12	SEG12	33BH	-	-	SEG12	SEG12
30CH	SEG13	SEG13	SEG13	SEG13	33CH	-	-	SEG13	SEG13
30DH	SEG14	SEG14	SEG14	SEG14	33DH	-	-	SEG14	SEG14
30EH	SEG15	SEG15	SEG15	SEG15	33EH	-	-	SEG15	SEG15
30FH	SEG16	SEG16	SEG16	SEG16	33FH	-	-	SEG16	SEG16
310H	SEG17	SEG17	SEG17	SEG17	340H	-	-	SEG17	SEG17
311H	SEG18	SEG18	SEG18	SEG18	341H	-	-	SEG18	SEG18

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM4	COM3	COM2	COM1		-	-	COM6	COM5
312H	SEG19	SEG19	SEG19	SEG19	342H	-	-	SEG19	SEG19
313H	SEG20	SEG20	SEG20	SEG20	343H	-	-	SEG20	SEG20
314H	SEG21	SEG21	SEG21	SEG21	344H	-	-	SEG21	SEG21
315H	SEG22	SEG22	SEG22	SEG22	345H	-	-	SEG22	SEG22
316H	SEG23	SEG23	SEG23	SEG23	346H	-	-	SEG23	SEG23
317H	SEG24	SEG24	SEG24	SEG24	347H	-	-	SEG24	SEG24
318H	SEG25	SEG25	SEG25	SEG25	348H	-	-	SEG25	SEG25
319H	SEG26	SEG26	SEG26	SEG26	349H	-	-	SEG26	SEG26
31AH	SEG27	SEG27	SEG27	SEG27	34AH	-	-	SEG27	SEG27
31BH	SEG28	SEG28	SEG28	SEG28	34BH	-	-	SEG28	SEG28
31CH	SEG29	SEG29	SEG29	SEG29	34CH	-	-	SEG29	SEG29
31DH	SEG30	SEG30	SEG30	SEG30	34DH	-	-	SEG30	SEG30
31EH	SEG31	SEG31	SEG31	SEG31	34EH	-	-	SEG31	SEG31
31FH	SEG32	SEG32	SEG32	SEG32	34FH	-	-	SEG32	SEG32
320H	SEG33	SEG33	SEG33	SEG33	350H	-	-	SEG33	SEG33
321H	SEG34	SEG34	SEG34	SEG34	351H	-	-	SEG34	SEG34
322H	SEG35	SEG35	SEG35	SEG35	352H	-	-	SEG35	SEG35
323H	SEG36	SEG36	SEG36	SEG36	353H	-	-	SEG36	SEG36
324H	SEG37	SEG37	SEG37	SEG37	354H	-	-	SEG37	SEG37
325H	SEG38	SEG38	SEG38	SEG38	355H	-	-	SEG38	SEG38

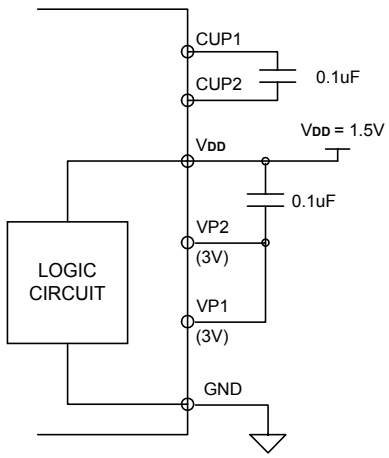
12.3. Connection Diagram

The pump circuit frequency could be 2k and 4k (selected by Code Option).

1. V_{DD} = 1.5V, 4.5V LCD, 1/6 duty, 1/3 bias
   and 1/5 duty, 1/3 bias
   and 1/4 duty, 1/3 bias

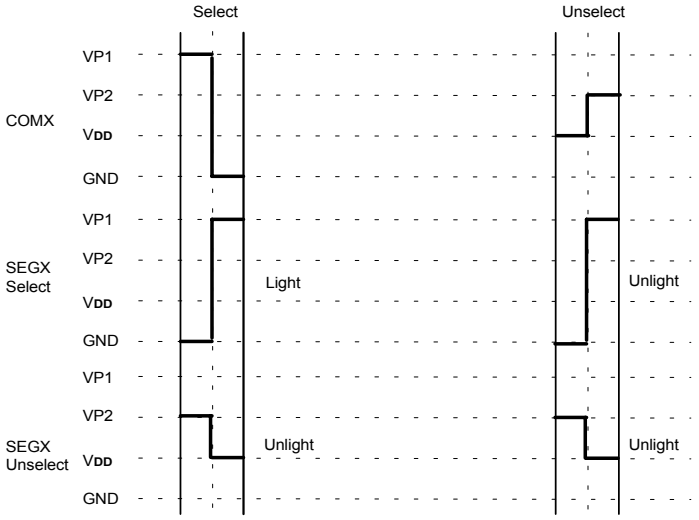


2. V_{DD} = 1.5V, 3V LCD, 1/3 duty, 1/2 bias

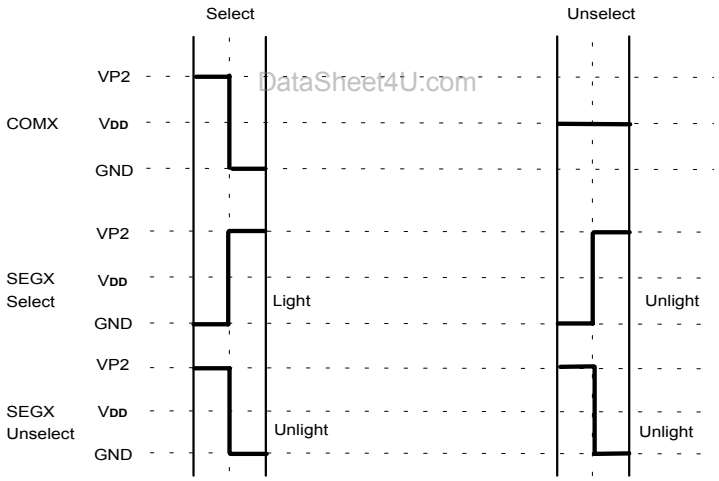


12.4. LCD Waveform

1/6, 1/5, 1/4 duty, 1/3 bias LCD waveform (V_{DD} = 1.5V, VP1 = 4.5V, VP2 = 3V)



1/3 duty, 1/2 bias LCD waveform (V_{DD} = 1.5V, VP1 = VP2 = 3V)



13. Interrupt

4 interrupt sources are available on SH67L19:

- External interrupt ($\overline{INT0}$ shared with PORTA.0)
- Timer0 interrupt (TM0INT)
- Base Timer interrupt (BTINT)
- PORTB & PORTC falling or rising edge detection interrupt ($\overline{INT1}$)

The configuration of interrupt's system register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	Remarks
$00	IEX	IET0	IEBT	IEP	1: Enable / 0: Disable
$01	IRQX	IRQT0	IRQBT	IRQP	1: Request / 0: No request

13.1. The Enable Flags and Request Flags

Both the Enable flags and Request flags can be read or written by software.
But the Request flags will be set to "1" by the hardware interrupt and the Enable flags will be reset by hardware when the interrupt service routine is entered.

13.2. Interrupt Servicing Sequence Diagram

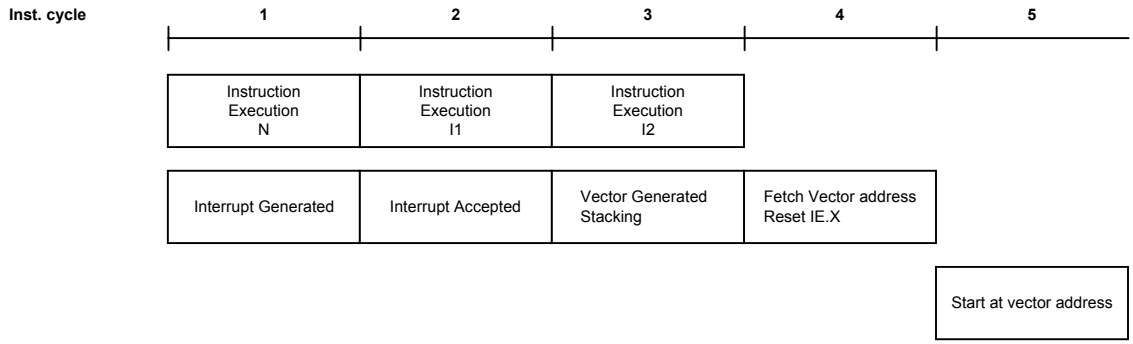
In SH6610C CPU interrupt services routine, the user can enable any interrupt enable flag before returning from an interrupt. The frequently asked question is when the next interrupt would be serviced? Will the nesting interrupt occur? From the servicing sequence timing diagram, if interrupt request is ready and instruction execution N is IE enable, then the interrupt can start right after the next two instructions: I1 or instruction I2 disable the interrupt request or enable flag, and then the interrupt service sequence would be terminated.

13.3. External Interrupt ($\overline{INT0}$)

External interrupt is shared with the PORTA.0 (falling or rising edge active). When the bit 3 of the register $0 (IEX) is set to "1", the external interrupt is enabled, and only PORTA.0 at input mode will generate external interrupt.

13.4. Timer 0 Interrupt (T0INT), Base Timer Interrupt (BTINT), Port Interrupt ($\overline{INT1}$)

If IET0 = 1, the overflow of timer 0 will create the interrupt of timer 0. If IEBT = 1, the overflow of the Base timer will create the interrupt of the Base timer. If IEP = 1, the falling or rising edge of every port in PORTB&C will create $\overline{INT1}$ interrupt (The condition is PORTB, C at input mode).

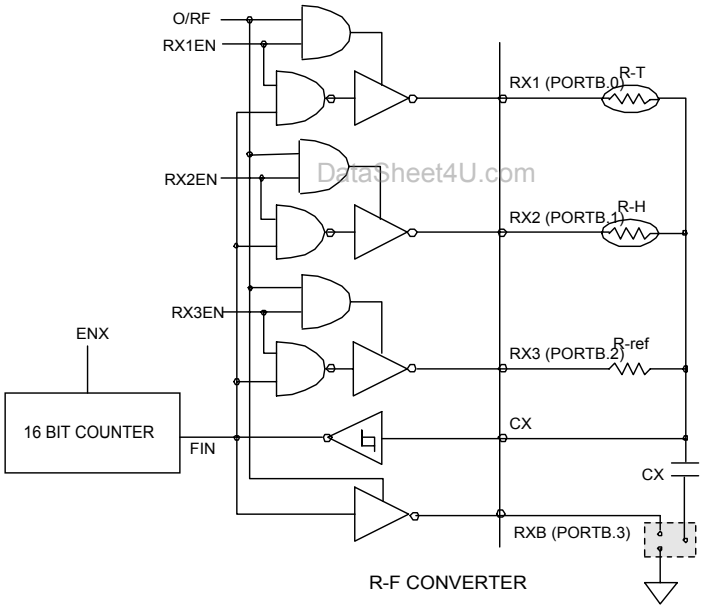


14. Resistor to Frequency Converter

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	Power On
$06	ENX	ELON	LCDOFF	PSGON	R/W	… Bit3: R-F convert counter on/off control	0010
$07	O/RF	RX3EN	RX2EN	RX1EN	R/W	Bit0 - 2: count resister1 - 3 enable Bit3: set PORTB as R-F converter	0000
$269	RF1.3	RF1.2	RF1.1	RF1.0	R/W	R-F counter register nibble 1 (bit0 - 3)	0000
$26A	RF2.3	RF2.2	RF2.1	RF2.0	R/W	R-F counter register nibble 2 (bit4 - 7)	0000
$26B	RF3.3	RF3.2	RF3.1	RF3.0	R/W	R-F counter register nibble 3 (bit8 - 11)	0000
$26C	RF4.3	RF4.2	RF4.1	RF4.0	R/W	R-F counter register nibble 4 (bit12 - 15)	0000
$26D	RF5.3	RF5.2	RF5.1	RF5.0	R/W	R-F counter register nibble 5 (bit16 - 19)	0000

When we set O/RF = 1, Port B is used as R-F converter. It's like a RC oscillation circuit, and uses the 20-bit counter to get the resistive value of the sensor. First to set RX1EN = 1 (enable RX1-F convert), and then start timer1 or timer0 counter and set ENX = 1 (start R-F counter). When the timer INT occurs, we can get the value of the RX1-F counter. So, we can get different count values of R-T, R-H, R-ref by setting RX1EN, RX2EN, RX3EN = 1 in turn.

The R-F converter could keep on working in HALT mode, and would stop automatically when the "STOP" instruction is executed. (Keep the last state of RX1-3 ports and stop the R-F counter.)



R-F CONVERTER

The SH67L19 provides two methods for R-F's application to improve the performance of R-F applications (selected by Code Option). When designing the R-F's peripheral circuit, we can select the capacitor connected with CX and PORTB.3 or CX and GND. Note: the method of the capacitor connection must match the corresponding Code Option.

Temperature sensor resistor: 10k - 50k @25℃ (for reference only)

Humidity sensor: 60k @25℃, 50%RH (for reference only)

Notice:

1. When the O/RF is set to “1”, PORTB interrupt will be disabled.
2. Connect CX to V_{DD} or GND when the R-F converter is not used.
3. The 20-bit counter can be used as an event counter when not using the R-F converter.
4. Max-frequency of R-F converter should be less than 2MHz.

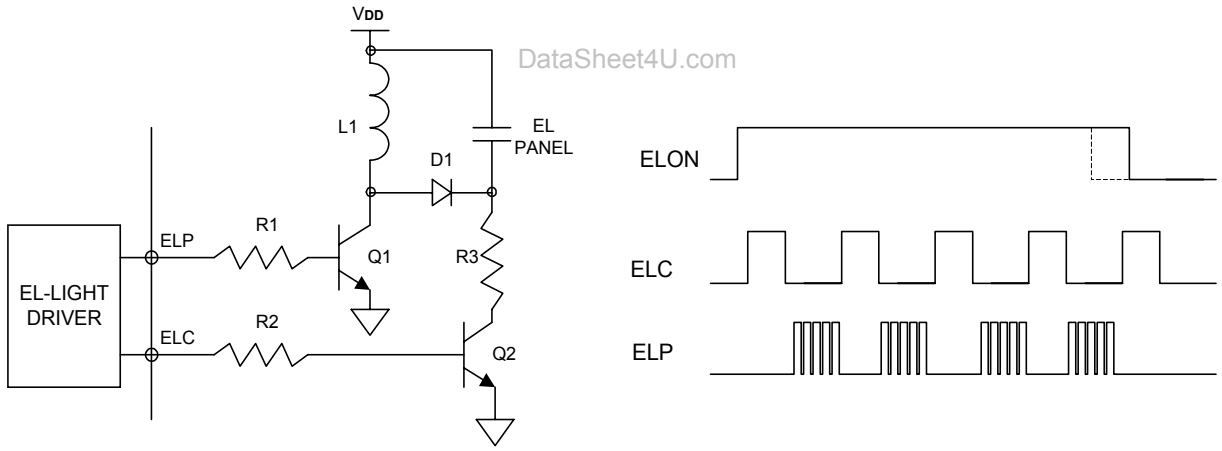
15. EL-LIGHT

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	Power On
$06	ENX	ELON	LCDOFF	PSGON	R/W	Bit0: PSG on/off control Bit1: LCD on/off control Bit2: EL-light on/off control Bit3: R-F convert counter on/off control	0010
$13	ELF	ELPF	HLM	S/CX	R/W	Bit0: Set CX as LCD segment 38 Bit1: Select LCD segment output high or low EL-LIGHT mode control Bit2: ELP driver output frequency control Bit3: EL-LIGHT driver frequency select	0001

ELPF: (frequency of ELP pin charge waveform)
0 ELCLK
1 ELCLK/2
(ELCLK = 32kHz@32kHz Oscillator or 131kHz/4@131kHz RC Oscillator by Code Option.)

ELF: (frequency of ELC pin discharge waveform)
0 ELCLK/64
1 ELCLK/32

Set the system register $13 to select the EL-LIGHT driver waveform. Setting ELON = 1 will turn on the EL-LIGHT driver. The ELC and ELP will output driver waveform automatically as shown in the following diagram. With externally transistor, diode, inductance and resistor, we can pump the EL panel to AC 100 - 250V.



ELP: Output for EL charge
ELC: Output for EL discharge

While the EL-LIGHT is turned on, the ELC will be turned on before ELP is on. When the EL-LIGHT is turned off, the ELP will turn off first, then ELC will still work for one cycle to make sure that there is no voltage left on EL panel.
The EL-LIGHT would keep on working in HALT mode. But it would turn off after the “STOP" instruction is executed (ELC & ELP keep low).

Notice:

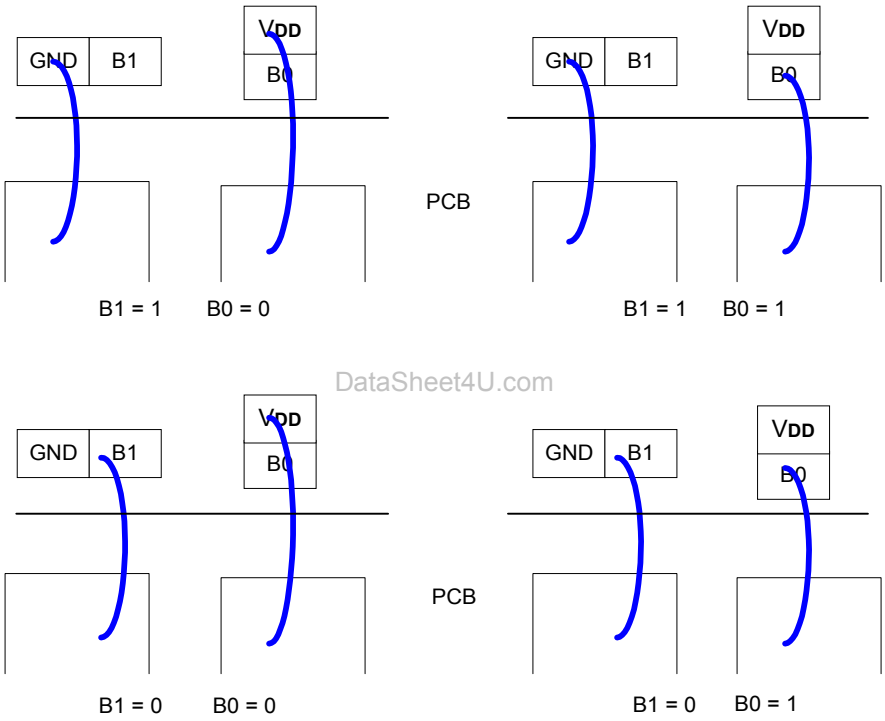
1. When PORTA.0 and PORTA.3 are used as EL drivers, the data of PA.0 & PA.3 must be clear to “0”.
2. Please turn on the HLM (heavy-load mode) before turning on the EL-LIGHT.
3. Please turn off the EL-LIGHT before executing the “STOP” instruction.

16. Options

Bonding options

System registers $15 bit1, bit0 are reserved for users. It is available for system developer to select 2 bonding options, and the user programs to select a subprogram.

B1	B0	Remarks	R/W
0	0	B1 bond to GND	R
1	0		R
0	1	B1 bond to GND and B0 bond to V_{DD}	R
1	1	B0 bond to V_{DD}	R



SH67L19 Bonding Option

17. STOP/HALT Mode

STOP/HALT Mode	Oscillator	CPU core	Wake up	Executing after Wake up
STOP (STOP instruction)	OSC stop OSCX Stop	Hold	RESET, $\overline{INT0}$, $\overline{INT1}$	(a) If RESET signal valid, system will reset. (b) If $\overline{INT0}$, $\overline{INT1}$ signal valid, system will enter interrupt subroutine, then execute the main program to continue.
HALT (HALT instruction)	OSC active OSCX active if OSCX is on	Hold	RESET, $\overline{INT0}$, T0IN, $\overline{INT1}$, BTINT	(a) If RESET signal valid, system will reset. (b) If $\overline{INT0}$, $\overline{INT1}$, T0INT, BTINT signal valid, system will enter interrupt subroutine first, then execute the main program to continue.

18. Instruction Set

All instructions are one-cycle and one-word instructions with characteristic in memory-oriented operation.
Arithmetic and Logical Instruction

Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + Ac + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx ← Mx + Ac + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + Ac	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx ← Mx + Ac	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -Ac + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx ← Mx + -Ac + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -Ac + 1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx ← Mx + -Ac + 1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ Ac	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx ← Mx ⊕ Ac	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | Ac	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx ← Mx | Ac	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & Ac	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx ← Mx & Ac	
SHR	11110 0000 000 0000	0 → AC [3] ; AC [0] → CY ; AC shift right one bit	CY

Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I + 1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I + 1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

Decimal Adjust

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC; Mx ←Decimal adjust for add.	CY
DAS X	11001 1010 xxx xxxx	AC; Mx ←Decimal adjust for sub.	CY

Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx ← I	

Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY; PC + 1 PC ← X (Not include p)	
RTNW H, L	11010 000h hhh llll	PC ← ST; TBR ← hhhh; AC ← llll	
RTNI	11010 1000 000 0000	CY; PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-C8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where

PC	Program counter	I	Immediate data	p	ROM page = 0
AC	Accumulator	⊕	Logical exclusive OR	ST	Stack
-AC	Complement of accumulator	|	Logical OR	TBR	Table Branch Register
CY	Carry flag	&	Logical AND		
Mx	Data memory	bbb	RAM bank = 000		

Absolute Maximum Rating*

DC Supply Voltage . . . . . -0.3V to +3.0V

Input Voltage . . . . . -0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . .. -10℃ to +60℃

Storage Temperature . . . . . -55℃ to +125℃

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability

DC Electrical Characteristics

DC Electrical Characteristics

(V_{DD} = 1.5V, GND = 0V, TA =25°C, fosc = 32.768kHz crystal, foscx is off, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	1.2	1.5	1.7	V	-
Operating Current	I_{OP}	-	4	6	μA	All output pins unload execute NOP instruction, exclude LCD, EL, PSG, R-F & Alarm current
Standby Current 1	I_{SB1}	-	2	3	μA	All output pins unload (HALT mode) exclude LCD current. (Not in heavy load mode)
Standby Current 2	I_{SB2}	-	-	0.5	μA	All output pins unload (STOP mode), LCD off
Input High Voltage	V_{IH1}	0.8 X V_{DD}	-	V_{DD} + 0.3	V	PORTA - PORTF, OSCI, OSCXI (Driven by external clock) (reference only)
Input High Voltage	V_{IH2}	0.85 X V_{DD}	-	V_{DD} + 0.3	V	$\overline{INT0}$, $\overline{RESET}$, TEST, CX (schmitt trigger input)
Input Low Voltage	V_{IL1}	GND - 0.3	-	0.2 X V_{DD}	V	PORTA - PORTF, OSCI, OSCXI (Driven by external clock) (reference only)
Input Low Voltage	V_{IL2}	GND - 0.3	-	0.15 X V_{DD}	V	$\overline{INT0}$, $\overline{RESET}$, TEST, CX, (schmitt trigger input)
Output High Voltage	V_{OH1}	0.8 X V_{DD}	-	-	V	PORTC - PORTF (I_{OH} = -0.3mA)
Output Low Voltage	V_{OL1}	-	-	0.2 X V_{DD}	V	PORTC - PORTF (I_{OL} = 0.3mA)
Output High Voltage	V_{OH2}	0.8 X V_{DD}	-	-	V	PORTA.1, PORTA.2 as PSG output, PORTA.0, PORTA.3 as EL driver, I_{OH} = -0.3mA
Output Low Voltage	V_{OL2}	-	-	0.2 X V_{DD}	V	PORTA.1, PORTA.2 as PSG output, PORTA.0, PORTA.3 as EL driver, I_{OL} = 0.3mA
Output High Voltage	V_{OH3}	0.8 X V_{DD}	-	-	V	PORTB as R-F (I_{OH} = -2.4mA) V_{DD}=1.2V
Output Low Voltage	V_{OL3}	-	-	0.2 X V_{DD}	V	PORTB as R-F (I_{OL} = 2.4mA) V_{DD}=1.2V
Output High Voltage	V_{OH4}	V_{P1} - 0.2	-	-	V	SEGX, I_{OH} = -3μA
Output Low Voltage	V_{OL4}	-	-	0.2	V	SEGX, I_{OL} = 3μA
Output High Voltage	V_{OH5}	V_{P1} - 0.2	-	-	V	COMX, I_{OH} = -8μA
Output Low Voltage	V_{OL5}	-	-	0.2	V	COMX, I_{OL} = 8μA
Pull-high/pull-low Resistor	R_{P1}	-	150	-	kΩ	Pull-high/pull-low resistor for PORT (I_{OH} = -6μA; I_{OL} = 6μA)
Pull-high Resistor	R_{P2}	-	250	-	kΩ	Pull-high resistor for RESET pin
LCD Lighting	I_{LCD}	-	-	1	μA	No panel loaded. LCD pump frequency = 4k

DC Electrical Characteristics

(V_{DD} = 1.5V, GND = 0V, TA = 25°C, fosc = 131kHz RC, foscx is off, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	1.2	1.5	1.7	V	-
Operating Current	I_{OP}	-	7	10	μA	All output pins unload execute NOP instruction, exclude LCD, EL, PSG, R-F & Alarm current
Standby Current	I_{SB1}	-	3	5	μA	All output pins unload (HALT mode) exclude LCD current. (Not in heavy load mode)
Standby Current	I_{SB2}	-	-	0.5	μA	All output pins unload (STOP mode), LCD off
Reset Current	I_{REST}	-	-	20	μA	Reset current

DC Electrical Characteristics

(V_{DD} = 1.5V, GND = 0V, TA = 25°C, foscx = 500kHz RC or 455kHz ceramic, fosc is on, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	1.2	1.5	1.7	V	-
Operating Current	I_{OP}	-	30	50	μA	All output pins unload execute NOP instruction, exclude LCD, EL, PSG, R-F & Alarm current
Standby Current	I_{SB1}	-	20	25	μA	All output pins unload (HALT mode) exclude LCD current. (Not heavy load mode)
Standby Current	I_{SB2}	-	-	0.5	μA	All output pins unload (STOP mode), LCD off

AC Characteristics

(V_{DD} = 1.5V, GND = 0V, TA = 25°C, fosc = 32.768kHz crystal, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Oscillation Start Time	t_{OST}	-	1	2	s	-

AC Characteristics

(V_{DD} = 1.5V, GND = 0V, TA = 25°C, fosc = 131kHz RC, unless otherwise specified)

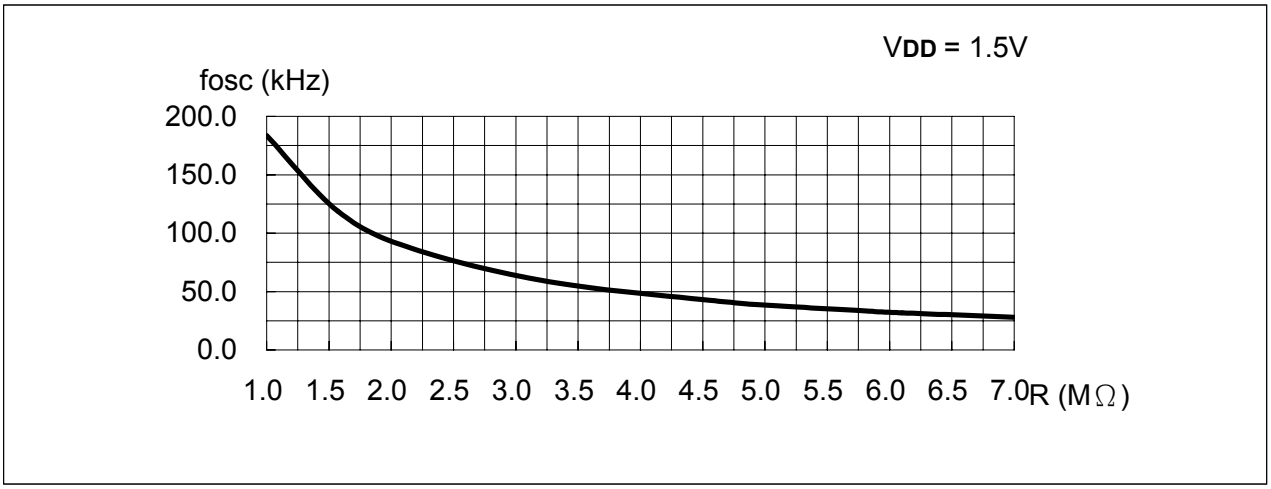
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Frequency Variation (RC)	Δ f/f	-	-	± 30	%	Include supply voltage and chip to chip variation

AC Characteristics

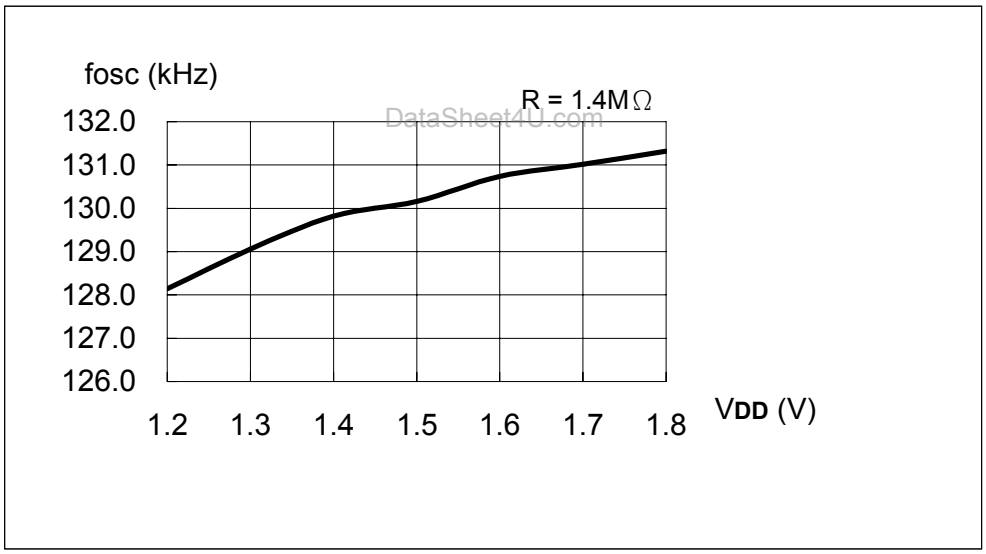
(V_{DD} = 1.5V, GND = 0V, TA = 25°C, foscx = 500kHz RC, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Frequency Variation (RC)	Δ f/f	-	-	± 30	%	Include supply voltage and chip to chip variation

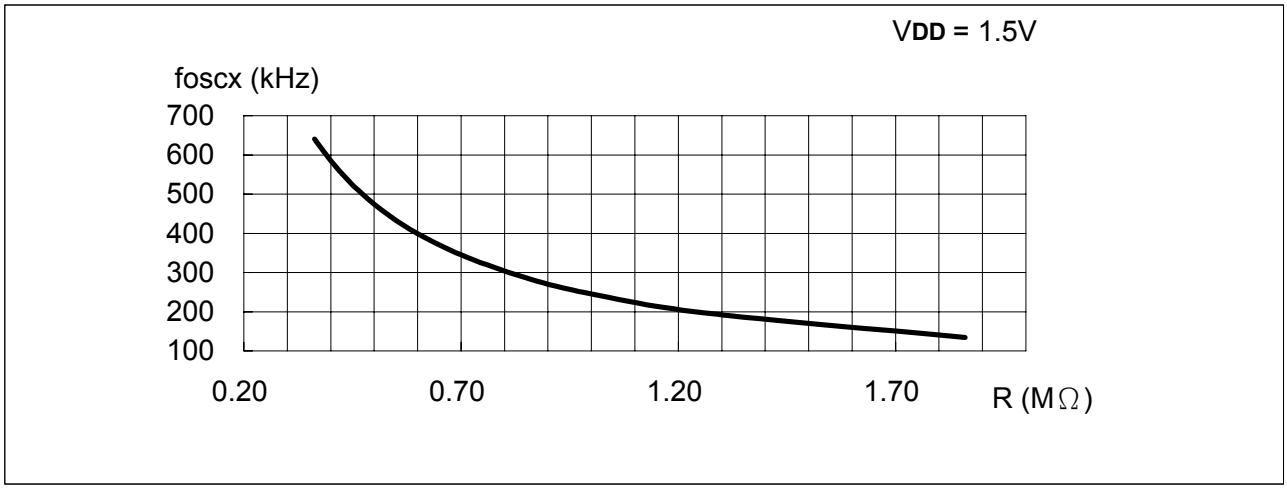
Typical RC Oscillator Resistor (OSC) vs. Frequency: (V_{DD} = 1.5V, for reference only)



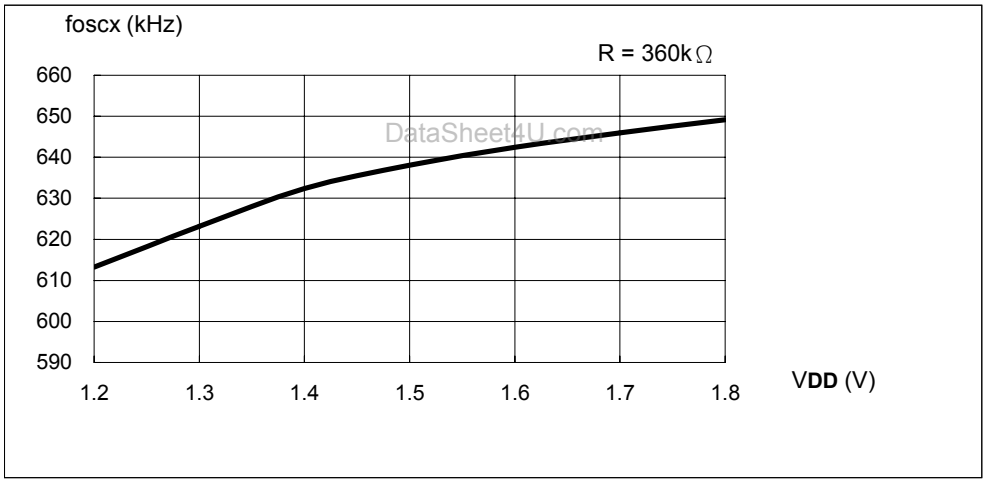
Typical V_{DD} vs. Frequency of RC Oscillator (OSC): (for reference only)



Typical RC Oscillator Resistor (OSCX) vs. Frequency: (V_{DD} = 1.5V, for reference only)



Typical V_{DD} vs. Frequency of RC Oscillator (OSCX): (for reference only)



Code Option:

Body data: 0110 1010 0000 1001 (67L19)

Data: CLDT PRAF 0000 0000

CL (OSC clock source)

0, 0: fosc = 32.768kHz Crystal (Default)

0, 1: fosc = 32kHz RC

1, x: fosc = 131kHz RC

DT (LCD duty selection)

0, 0: 1/6 duty (Default)

0, 1: 1/5 duty

1, 0: 1/4 duty

1, 1: 1/3 duty

P (LCD Pump circuit frequency)

0: 2kHz (Default)

1: 4kHz

R (internal pull high for RESET selection)

0: internal pull high enable (Default)

1: internal pull high disable

A (alarm carrier frequency)

0: 4kHz (Default)

1: 2kHz

F (R-F application's selection)

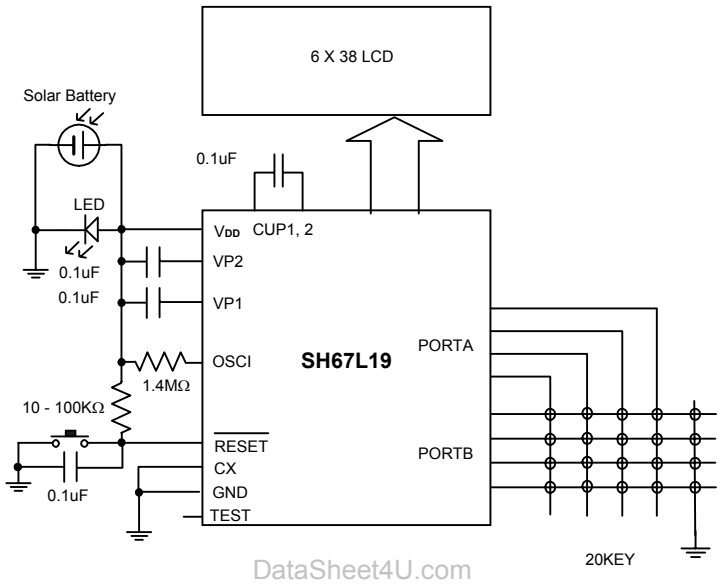
0: The capacitor connect with CX and PORTB.3 (Default)

1: The capacitor connect with CX and GND

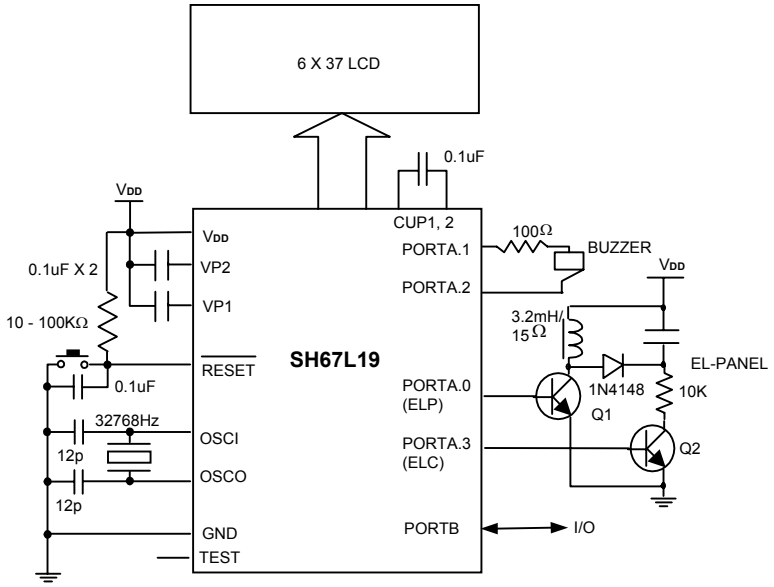
Application Circuits (for reference only)

SH67L19 chip substrate connects to system ground.

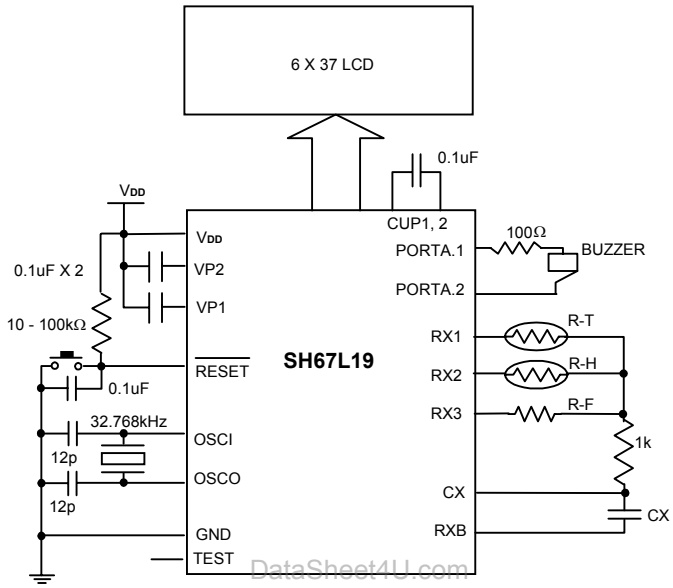
AP1: V_{DD} = 1.5V (Solar battery)
OSC: RC: 131kHz (Code Option)
LCD: 4.5V, 1/6 duty, 1/3 bias
PORTA, PORTB: I/O; PORTC - PORTF used as segment; CX used as segment



AP2: V_{DD} = 1.5V
OSC: 32.768kHz crystal (Code Option)
LCD: 4.5V, 1/6 duty, 1/3 bias
PORTA.1, PORTA.2: PSG output
PORTA.0, PORTA.3: EL-LIGHT driver
PORTB: I/O; CX, PORTC - PORTF: Segment

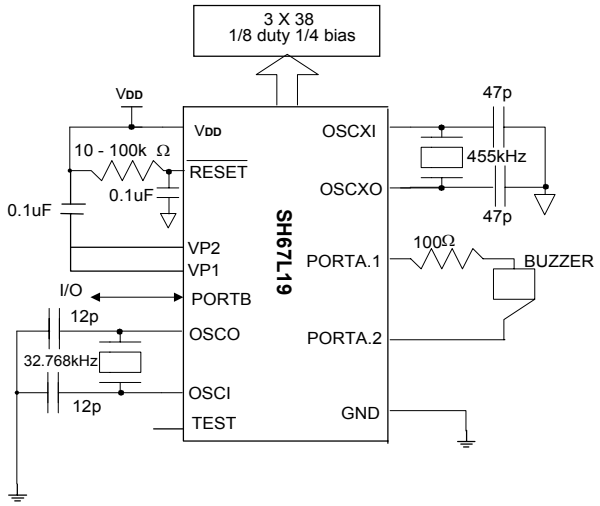


AP3: V_{DD} = 1.5V
OSC: 32.768kHz crystal (Code Option)
LCD: 4.5V, 1/6 duty, 1/3 bias
PORTA.1, PORTA.2: PSG output
PORTA.0, PORTA.3: I/O
PORTB, CX: R-F Converter
PORTC - PORTF: Segment

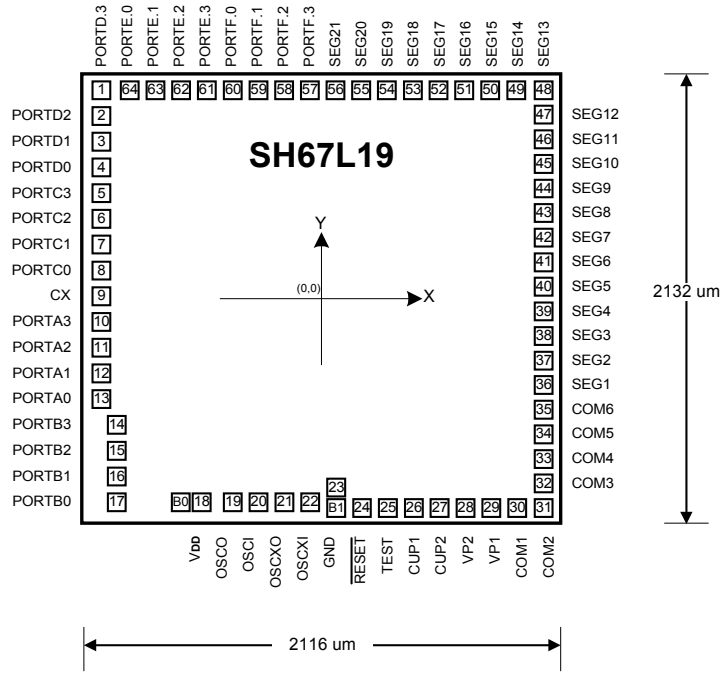


R-T: Temperature Sensor
R-H: Humidity Sensor
R-F: Reference Resister
CX: R-F converter capacitor

AP4: V_{DD} = 1.5V
OSC: Crystal oscillator 32.768kHz (Code Option)
OSCX: Ceramic oscillator 455kHz
PORTB: I/O; PORTA.1, PORTA.2: ALARM output
LCD: 3V, 1/3 duty, 1/2 bias



Bonding Diagram



Pad Location

unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	PORTD.3	-988	996	20	OSCI	-263	-964
2	PORTD.2	-988	866	21	OSCXO	-153	-964
3	PORTD.1	-988	749	22	OSCXI	-43	-964
4	PORTD.0	-988	632		B1	67	-996
5	PORTC.3	-988	515	23	GND	67	-896
6	PORTC.2	-988	398	24	$\overline{\text{RESET}}$	177	-996
7	PORTC.1	-988	281	25	TEST	289	-996
8	PORTC.0	-988	164	26	CUP1	401	-996
9	CX	-988	47	27	CUP2	513	-996
10	PORTA.3	-988	-70	28	VP2	625	-996
11	PORTA.2	-988	-187	29	VP1	737	-996
12	PORTA.1	-988	-304	30	COM1	857	-996
13	PORTA.0	-988	-421	31	COM2	988	-996
14	PORTB.3	-924.4	-562.8	32	COM3	988	-862.5
15	PORTB.2	-924.4	-703	33	COM4	988	-747.5
16	PORTB.1	-924.4	-818	34	COM5	988	-632.5
17	PORTB.0	-924.4	-958.2	35	COM6	988	-517.5
	B0	-603	-966	36	SEG1	988	-402.5
18	VDD	-503	-966	37	SEG2	988	-287.5
19	OSCO	-373	-964	38	SEG3	988	-172.5

Pad Location (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
39	SEG4	988	-57.5	52	SEG17	513	996
40	SEG5	988	57.5	53	SEG18	399	996
41	SEG6	988	172.5	54	SEG19	285	996
42	SEG7	988	287.5	55	SEG20	171	996
43	SEG8	988	402.5	56	SEG21	57	996
44	SEG9	988	517.5	57	PORTF.3	-57	996
45	SEG10	988	632.5	58	PORTF.2	-171	996
46	SEG11	988	747.5	59	PORTF.1	-285	996
47	SEG12	988	862.5	60	PORTF.0	-399	996
48	SEG13	988	996	61	PORTE.3	-513	996
49	SEG14	855	996	62	PORTE.2	-627	996
50	SEG15	741	996	63	PORTE.1	-741	996
51	SEG16	627	996	64	PORTE.0	-855	996

Ordering Information

Part No.	Package
SH67L19H	CHIP FORM

Data Sheet Revision History

Version	Content	Date
1.0	Original	Dec. 2004